2. An overflow is a _____
a) Hardware problem
b) Software problem
c) User input problem
d) Input Output Error

Answer: b

4. Logic circuitry is used to detect _____
a) Underflow
b) MSD
c) Overflow
d) LSD

Answer: c

8. Which one is used for logical manipulations?
a) 2’s complement
b) 9’s complement
c) 1’s complement
d) 10’s complement

Answer: c

9. For arithmetic operations only _____
a) 1’s complement is used
b) 2’s complement
c) 10’s complement
d) 9’s complement

Answer: b

1. In boolean algebra, the OR operation is performed by which properties?
a) Associative properties
b) Commutative properties
c) Distributive properties
d) All of the Mentioned

Answer: d
Explanation: The expression for Associative property is given by A+(B+C) = (A+B)+C & A*(B*C) = (A*B)*C.

The expression for Commutative property is given by A+B = B+A & A*B = B*A.
The expression for Distributive property is given by A+BC=(A+B)(A+C) & A(B+C) = AB+AC.

2. The expression for Absorption law is given by _____
a) A + AB = A
b) A + AB = B
c) AB + AA' = A
d) A + B = B + A

Answer: a
Explanation: The expression for Absorption Law is given by: A+AB = A.
Proof: A + AB = A(1+B) = A (Since 1 + B = 1 as per 1's Property).

3. According to boolean law: A + 1 = ?
a) 1
b) A
c) 0
d) A'

Answer: a
Explanation: A + 1 = 1, as per 1's Property.

4. The involution of A is equal to _____
a) A
b) A'
c) 1
d) 0

Answer: a
Explanation: The involution of A means double inversion of A (i.e. A") and is equal to A. Proof: ((A)')' = A

5. A(A + B) = ?
a) AB
b) 1
c) (1 + AB)
d) A

Answer: d
Explanation: A(A + B) = AA + AB (By Distributive Property) = A + AB (A.A = A By Commutative Property) = A(1 + B) = A*1 (1 + B = 1 by 1's Property) = A.

6. DeMorgan’s theorem states that _____
a) (AB)’ = A’ + B’
b) (A + B)’ = A’ * B
c) A’ + B’ = A’B’
d) (AB)’ = A’ + B

Answer: a
Explanation: The DeMorgan’s law states that (AB)’ = A’ + B’ & (A + B)’ = A’ * B’, as per the Dual Property.

7. (A + B)(A’ * B’) = ?
a) 1
b) 0
c) AB
d) AB’

Answer: b
Explanation: The DeMorgan’s law states that (AB)’ = A’ + B’ & (A + B)’ = A’ * B’, as per the Dual Property.

8. Complement of the expression A’B + CD’ is _____
a) (A’ + B)(C’ + D)
b) (A + B’)(C’ + D)
c) (A’ + B)(C’ + D)
d) (A + B’)(C + D’)

Answer: b
Explanation: (A’B + CD’)’ = (A’B)'(CD’)’ (By DeMorgan’s Theorem) = (A” + B’)(C’ + D”) (By DeMorgan’s Theorem) = (A + B’)(C’ + D).

9. Simplify Y = AB’ + (A’ + B)C.
a) AB’ + C
b) AB + AC
c) A’B + AC’
d) AB + A

Answer: a
Explanation: Y = AB’ + (A’ + B)C = AB’ + (AB’)’C = (AB’ + C)(AB’ + AB’) = (AB’ + C).1 = (AB’ + C).

10. The boolean function A + BC is a reduced form of _____
a) AB + BC
b) (A + B)(A + C)

c) A’B + AB’C
d) (A + C)B

Answer: b
Explanation: (A + B)(A + C) = AA + AC + AB + BC = A + AC + AB + BC (By Commutative Property) = A(1 + C + B) + BC = A + BC (1 + B + C =1 By 1’s Property).

1. The logical sum of two or more logical product terms is called _____
a) SOP
b) POS
c) OR operation
d) NAND operation

Answer: a
Explanation: The logical sum of two or more logical product terms, is called SOP (i.e. sum of product). The logical product of two or more logical sum terms is called POS (i.e. product of sums).

2. The expression Y=AB+BC+AC shows the _____ operation.
a) EX-OR
b) SOP
c) POS
d) NOR

Answer: b
Explanation: The given expression has the operation product as well as the sum of that. So, it shows SOP operation. POS will be the product of sum terms.

3. The expression Y=(A+B)(B+C)(C+A) shows the _____ operation.
a) AND
b) POS
c) SOP
d) NAND

Answer: b
Explanation: The given expression has the operation sum as well as the product of that. So, it shows POS(product of sum) operation. SOP will be the sum of product terms.

4. A product term containing all K variables of the function in either complemented or uncomplemented form is called a _____
a) Minterm
b) Maxterm
c) Midterm
d) ∑ term

Answer: a
Explanation: A product term containing all K variables of the function in either complemented or uncomplemented form is called a minterm. A sum term containing all K variables of the function in either complemented or uncomplemented form is called a maxterm.

5. According to the property of minterm, how many combination will have value equal to 1 for K input variables?
a) 0
b) 1
c) 2
d) 3

Answer: b
Explanation: The main property of a minterm is that it possesses the value 1 for only one combination of K input variables and the remaining will have the value 0.

6. The canonical sum of product form of the function y(A,B) = A + B is _____
a) AB + BB + A'A
b) AB + AB' + A'B
c) BA + BA' + A'B'
d) AB' + A'B + A'B'

Answer: b
Explanation: A + B = A.1 + B.1 = A(B + B') + B(A + A') = AB + AB' + BA +BA' = AB + AB' + A'B = AB + AB' + A'B.

7. A variable on its own or in its complement form is known as a _____
a) Product Term
b) Literal
c) Sum Term
d) Word

Answer: b
Explanation: A literal is a single logic variable or its complement. For example — X, Y, A', Z, X' etc.

8. Maxterm is the sum of _____ of the corresponding Minterm with its literal complement.
a) Terms
b) Words
c) Numbers
d) Nibble

Answer: a
Explanation: Maxterm is the sum of terms of the corresponding Minterm with its literal complemented.

9. Canonical form is a unique way of representing _____
a) SOP
b) Minterm
c) Boolean Expressions
d) POS

Answer: c
Explanation: Boolean Expressions are represented through a canonical form. An example of canonical form is A'B'C' + AB'C + ABC'.

10. There are _____ Minterms for 3 variables (a, b, c).
a) 0
b) 2
c) 8
d) 1

Answer: c
Explanation: Minterm is given by 2n. So, 23 = 8 minterms are required.

11. _____ expressions can be implemented using either (1) 2-level AND-OR logic circuits or (2) 2-level NAND logic circuits.
a) POS
b) Literals
c) SOP
d) POS

Answer: c
Explanation: SOP expressions can be implemented using either (1) 2-level AND-OR logic circuits or (2) 2-level NAND logic circuits.

1. A Karnaugh map (K-map) is an abstract form of _____ diagram organized as a matrix of squares.
a) Venn Diagram
b) Cycle Diagram
c) Block diagram
d) Triangular Diagram

Answer: a
Explanation: A Karnaugh map (K-map) is an abstract form of Venn diagram organized as a matrix of squares, where each square represents a Maxterm or a Minterm.

2. There are _____ cells in a 4-variable K-map.
a) 12
b) 16
c) 18
d) 8

Answer: b
Explanation: There are 16 = (24) cells in a 4-variable K-map.

3. The K-map based Boolean reduction is based on the following Unifying Theorem: A + A' = 1.
a) Impact
b) Non Impact
c) Force
d) Complementarity

Answer: b
Explanation: The given expression A +A' = 1 is based on non-impact unifying theorem.

4. Each product term of a group, w'.x.y' and w.y, represents the _____ in that group.
a) Input
b) POS
c) Sum-of-Minterms
d) Sum of Maxterms

Answer: c
Explanation: In a minterm, each variable w, x or y appears once either as the variable itself or as the inverse. So, the given expression satisfies the property of Sum of Minterm.

5. The prime implicant which has at least one element that is not present in any other implicant is known as _____
a) Essential Prime Implicant
b) Implicant
c) Complement
d) Prime Complement

Answer: a
Explanation: Essential prime implicants are prime implicants that cover an output of the function that no combination of other prime implicants is able to cover.

6. Product-of-Sums expressions can be implemented using _____
a) 2-level OR-AND logic circuits
b) 2-level NOR logic circuits
c) 2-level XOR logic circuits
d) Both 2-level OR-AND and NOR logic circuits

Answer: d
Explanation: Product-of-Sums expressions can be implemented using 2-level OR-AND & NOR logic circuits.

7. Each group of adjacent Minterms (group size in powers of twos) corresponds to a possible product term of the given _____
a) Function
b) Value
c) Set
d) Word

Answer: a
Explanation: Each group of adjacent Minterms (group size in powers of twos) corresponds to a possible product term of the given function.

8. Don’t care conditions can be used for simplifying Boolean expressions in _____
a) Registers
b) Terms
c) K-maps
d) Latches

Answer: c
Explanation: Don’t care conditions can be used for simplifying Boolean expressions in K-maps which helps in pairing with 1/0.

9. It should be kept in mind that don’t care terms should be used along with the terms that are present in _____
a) Minterms
b) Expressions
c) K-Map
d) Latches

Answer: a
Explanation: It should be kept in mind that don’t care terms should be used along with the terms that are present in minterms as well as maxterms which reduces the complexity of the boolean expression.

10. Using the transformation method you can realize any POS realization of OR-AND with only.
a) XOR
b) NAND
c) AND
d) NOR

Answer: d
Explanation: Using the transformation method we can realize any POS realization of OR-AND with only NOR.

11. There are many situations in logic design in which simplification of logic expression is possible in terms of XOR and _____ operations.
a) X-NOR
b) XOR
c) NOR
d) NAND

Answer: a
Explanation: There are many situations in logic design in which simplification of logic expression is possible in terms of XOR and XNOR operations.
Expression of XOR : AB' + A'B
Expression of XNOR : AB + A'B'

12. These logic gates are widely used in _____ design and therefore are available in IC form.
a) Sampling
b) Digital
c) Analog
d) Systems

Answer: b
Explanation: These logic gates(XOR, XNOR, NOR) are widely used in digital design and therefore are available in IC form as digital circuits deal with data transmission in the form of binary digits.

13. In case of XOR/XNOR simplification we have to look for the following _____
a) Diagonal Adjacencies
b) Offset Adjacencies
c) Straight Adjacencies
d) Both diagonal and offset adjencies

Answer: d
Explanation: In case of XOR/XNOR simplification we have to look for the following diagonal and

offset adjacencies. XOR gives output 1 when odd number of 1s are present in input while XNOR gives output 1 when even number of 1s or all 0s are present in input.

14. Entries known as _____ mapping.
a) Diagonal
b) Straight
c) K
d) Boolean

Answer: a
Explanation: Entries known as diagonal mapping. The diagonal mapping holds true when for any relation, there is a projection of product on the factor.

1. The output of an EX-NOR gate is 1. Which input combination is correct?
a) A = 1, B = 0
b) A = 0, B = 1
c) A = 0, B = 0
d) A = 0, B' = 1

Answer: c
Explanation: The output of EX-NOR gate is given by AB + A'B'. So, for A = 0 and B = 0 the output will be 1.

2. In which of the following gates the output is 1 if and only if at least one input is 1?
a) AND
b) NOR
c) NAND
d) OR

Answer: d
Explanation: In or gate we need at least one bit to be equal to 1 to generate the output as 1 because OR means any of the condition out of two is equal to 1 which means if at least one input is 1 then it shows output as 1.

3. The time required for a gate or inverter to change its state is called _____
a) Rise time
b) Decay time
c) Propagation time
d) Charging time

Answer: c
Explanation: The time required for a gate or inverter to change its state is called propagation time.

4. What is the minimum number of two input NAND gates used to perform the function of two input OR gates?
a) One
b) Two
c) Three
d) Four

Answer: c
Explanation: Y = A + B. This is the equation of OR gate. We require 3 NAND gates to create OR gate. We can also write,
1st, 2nd and 3rd NAND operations as: Y = ((NOT A) AND (NOT B))' = A'' + B'' = (A+B).

5. Odd parity of word can be conveniently tested by _____
a) OR gate
b) AND gate
c) NAND gate
d) XOR gate

Answer: d
Explanation: Odd parity of word can be conveniently tested by XOR gate, since, XOR outputs 1 only when the input has odd number of 1's.

6. The number of full and half adders are required to add 16-bit number is _____
a) 8 half adders, 8 full adders
b) 1 half adders, 15 full adders
c) 16 half adders, 0 full adders
d) 4 half adders, 12 full adders

Answer: b
Explanation: Half adder has two inputs and two outputs whereas Full Adder has 3 inputs and 2 outputs. One half adder can add the least significant bit of the two numbers whereas full adders are required to add the remaining 15 bits as they all involve adding carries.

7. Which of the following will give the sum of full adders as output?
a) Three point major circuit
b) Three bit parity checker
c) Three bit comparator
d) Three bit counter

Answer: d
Explanation: Counters are used for counting purposes in ascending or descending order. Three bit counter will give the sum of full adders as output.

8. Which of the following gate is known as coincidence detector?
a) AND gate
b) OR gate
c) NOR gate
d) NAND gate

Answer: a
Explanation: AND gate is known as coincidence detector due to multiplicity behaviour, as it outputs 1 only when all the inputs are 1.

9. An OR gate can be imagined as _____
a) Switches connected in series
b) Switches connected in parallel
c) MOS transistor connected in series
d) BJT transistor connected in series

Answer: b
Explanation: OR gate means addition of two inputs, which outputs when any of the input is high. Due to this reason, it is imagined as switches connected in parallel.

10. How many full adders are required to construct an m-bit parallel adder?
a) m/2
b) m
c) m-1
d) m+1

Answer: c
Explanation: We need adder for every bit. So we should need m bit adders. A full adder adds a carry bit to two inputs and produces an output and a carry. But the most significant bits can use a half adder which differs from the full adder as in that it has no carry input, so we need m-1 full adders and 1 half adder in m bit parallel adder.

2. The code where all successive numbers differ from their preceding number by single bit is _____
a) Alphanumeric Code
b) BCD
c) Excess 3
d) Gray

Answer: d
Explanation: The code where all successive numbers differ from their preceding number by single bit is gray code. It is an unweighted code. The most important characteristic of this code is that only a single bit change occurs when going from one code number to next. BCD Code is one in which

decimal digits are represented by a group of 4-bits each, whereas, in Excess-3 Code, the decimal numbers are incremented by 3 and then written in their BCD format.

3. The following switching functions are to be implemented using a decoder:
f1 = ∑m(1, 2, 4, 8, 10, 14) f2 = ∑m(2, 5, 9, 11) f3 = ∑m(2, 4, 5, 6, 7)
The minimum configuration of decoder will be _____
a) 2 to 4 line
b) 3 to 8 line
c) 4 to 16 line
d) 5 to 32 line

Answer: c
Explanation: 4 to 16 line decoder as the minterms are ranging from 1 to 14.

4. How many AND gates are required to realize Y = CD + EF + G?
a) 4
b) 5
c) 3
d) 2

Answer: d
Explanation: To realize Y = CD + EF + G, two AND gates are required and two OR gates are required.

5. The NOR gate output will be high if the two inputs are _____
a) 00
b) 01
c) 10
d) 11

Answer: a
Explanation: In 01, 10 or 11 output is low if any of the I/P is high. So, the correct option will be 00.

6. How many two-input AND and OR gates are required to realize Y = CD+EF+G?
a) 2, 2
b) 2, 3
c) 3, 3
d) 3, 2

Answer: a
Explanation: Y = CD + EF + G

The number of two input AND gate = 2
The number of two input OR gate = 2.

7. A universal logic gate is one which can be used to generate any logic function. Which of the following is a universal logic gate?
a) OR
b) AND
c) XOR
d) NAND

Answer: d
Explanation: An Universal Logic Gate is one which can generate any logic function and also the three basic gates: AND, OR and NOT. Thus, NOR and NAND can generate any logic function and are thus Universal Logic Gates.

8. A full adder logic circuit will have _____
a) Two inputs and one output
b) Three inputs and three outputs
c) Two inputs and two outputs
d) Three inputs and two outputs

Answer: d
Explanation: A full adder circuit will add two bits and it will also accounts the carry input generated in the previous stage. Thus three inputs and two outputs (Sum and Carry) are there. In case of half adder circuit, there are only two inputs bits and two outputs (SUM and CARRY).

9. How many two input AND gates and two input OR gates are required to realize Y = BD + CE + AB?
a) 3, 2
b) 4, 2
c) 1, 1
d) 2, 3

Answer: a
Explanation: There are three product terms. So, three AND gates of two inputs are required. As only two input OR gates are available, so two OR gates are required to get the logical sum of three product terms.

10. Which of the following are known as universal gates?
a) NAND & NOR
b) AND & OR
c) XOR & OR
d) EX-NOR & XOR

Answer: a
Explanation: The NAND & NOR gates are known as universal gates because any digital circuit can be realized completely by using either of these two gates, and also they can generate the 3 basic gates AND, OR and NOT.

11. The gates required to build a half adder are _____
a) EX-OR gate and NOR gate
b) EX-OR gate and OR gate
c) EX-OR gate and AND gate
d) EX-NOR gate and AND gate

Answer: c
Explanation: The gates required to build a half adder are EX-OR gate and AND gate. EX-OR outputs the SUM of the two input bits whereas AND outputs the CARRY of the two input bits.

1. A single transistor can be used to build which of the following digital logic gates?
a) AND gates
b) OR gates
c) NOT gates
d) NAND gates

Answer: c
Explanation: A transistor can be used as a switch. That is when base is low collector is high (input zero, output one) and base is high collector is low (input 1, output 0).

2. How many truth table entries are necessary for a four-input circuit?
a) 4
b) 8
c) 12
d) 16

Answer: d
Explanation: For 4 inputs: 24 = 16 truth table entries are necessary.

3. Which input values will cause an AND logic gate to produce a HIGH output?
a) At least one input is HIGH
b) At least one input is LOW
c) All inputs are HIGH
d) All inputs are LOW

Answer: c
Explanation: For AND gate, the output is high only when both inputs are high. That’s why the high

output in AND will occurs only when all the inputs are high. However, in case of OR gate, if atleast one input is high, the output will be high.

4. Exclusive-OR (XOR) logic gates can be constructed from what other logic gates?
a) OR gates only
b) AND gates and NOT gates
c) AND gates, OR gates, and NOT gates
d) OR gates and NOT gates

Answer: c
Explanation: Expression for XOR is: A.(B')+(A').B
So in the above expression, the following logic gates are used: AND, OR, NOT.
Thus, 2 AND gates with two-inputs and 1 OR gate with two-inputs will be required for constructing a XOR gate.

5. The basic logic gate whose output is the complement of the input is the _____
a) OR gate
b) AND gate
c) INVERTER gate
d) XOR gate

Answer: c
Explanation: It is also called NOT gate and it simply inverts the input, such that 1 becomes 0 and 0 becomes 1.

6. The AND function can be used to _____ and the OR function can be used to _____
a) Enable, disable
b) Disable, enable
c) Synchronize, energize
d) Detect, invert

Answer: a
Explanation: The AND gate and OR gate are used for enabling and disabling respectively because of their multiplicity and additivity property. The AND gate outputs 1 when all inputs are at logic 1, whereas the OR gate outputs 0 when all inputs are at logic 0.

7. The dependency notation ">=1" inside a block stands for which operation?
a) OR
b) XOR
c) AND
d) XNOR

Answer: a
Explanation: The dependency notation “>=1” inside a block stands for OR operation.

8. If we use an AND gate to inhibit a signal from passing one of the inputs must be _____
a) LOW
b) HIGH
c) Inverted
d) Floating

Answer: a
Explanation: AND gate means A*B and OR gate means A+B and to inhibit means to get low signal, one of the input must be low. It means (0*1=0 or 1*0=0) we will get low output signal. Thus, AND gate outputs 1 only when all inputs are at logic level 1 else it outputs 0.

9. Logic gate circuits contain predictable gate functions that open theirs _____
a) Outputs
b) Inputs
c) Pre-state
d) Impedance state

Answer: b
Explanation: Logic gate circuits contain predictable gate functions that open their inputs because we are free to give any types of inputs.

10. How many NAND circuits are contained in a 7400 NAND IC?
a) 1
b) 2
c) 4
d) 8

Answer: c
Explanation: 7400 IC’s pin has total 14 pin. Pin no 7 use for GND and pin no 14 used for +vcc and remaining pins used for connections. For a NAND gate two inputs are required and one output is obtained means for NAND gate 3 pin connections are required. Thus, a 7400IC contains 4 NAND gates with each having 3 pins. Therefore, total 12 pins dedicated for the NAND operation. Rest 2 pins for power supply.

1. SSI refers to _____
a) Small Scale Integration

2. Small Scale Integration(SSI) refers to ICs with _____ gates on the same chip.
a) Fewer than 10
b) Greater than 10

c) Equal to 10
d) Greater than 50

Answer: a

—

Explanation: MSI means Medium Scale Integration.
Medium Scale Integration includes 12 to 100 gates per chip.

—
6. Integrated circuits are classified as _____
a) Large, Small and Medium
b) Very Large, Small and Linear
c) Linear and Digital
d) Non-Linear and Digital

Answer: c
Explanation: Integrated circuits are classified as Linear and Digital. Linear operates with continuous and digital refers to discrete signals.

7. According to the IC fabrication process logic families can be divided into two broad categories as _____
a) RTL and TTL
b) HTL and MOS
c) ECL and DTL
d) Bipolar and MOS

Answer: d
Explanation: According to the IC fabrication process logic families can be divided into two broad categories as: Bipolar and Metal-oxide semiconductor. The mentioned all others are part of bipolar. Bipolar IC fabrication refers to TTL logic where MOS refers to CMOS logic.

—-
The full form of DIP is Dual-in-Line Package.
—

LCC refers to Leadless Chip Carrier.
—
Explanation: Metal Oxide Semiconductor families includes PMOS, NMOS and CMOS.
—
6. Which of the following combinations of logic gates can decode binary 1101?
a) One 4-input AND gate

b) One 4-input AND gate, one inverter
c) One 4-input AND gate, one OR gate
d) One 4-input NAND gate, one inverter

Answer: b
Explanation: For decoding any number output must be high for that code and this is possible in One 4-input AND gate, one inverter option only. We can have 1st, 2nd and 4th bit high and supplied to the AND gate and the 3rd bit (low) going through inverter 1st and then going to the AND gate. A decoder is a combinational circuit that converts binary data to n-coded data upto 2n outputs.

9. The carry propagation can be expressed as _____
a) Cp = AB
b) Cp = A + B
c) All but Y0 are LOW
d) All but Y0 are HIGH

Answer: b
Explanation: This happens in parallel adders (where we try to add numbers in parallel via more than one adders). A carry propagation occurs when carry from one adder needs to be forwarded to other adder and that second adder is holding the computation (addition) because carry from first adder has not come yet. So, there is a slight delay for second adder and this is known as carry propagation.

10. 3 bits full adder contains _____
a) 3 combinational inputs
b) 4 combinational inputs
c) 6 combinational inputs
d) 8 combinational inputs

Answer: d
Explanation: Full Adder is a combinational circuit with 3 input bits and 2 output bits CARRY and SUM. Three bits full adder requires 23 = 8 combinational circuits.

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A multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line, depending on the active select lines.

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Data Selector is another name of Multiplexer. A multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line, depending on the active select lines.

—-

14. The enable input is also known as _____
a) Select input
b) Decoded input
c) Strobe
d) Sink

Answer: c
Explanation: The enable input is also known as strobe which is used to cascade two or more multiplexer ICs to construct a multiplexer with a larger number of inputs. Enable input activates the multiplexer to operate.

12. How many NOT gates are required for the construction of a 4-to-1 multiplexer?
a) 3
b) 4
c) 2
d) 5

Answer: c
Explanation: There are two NOT gates required for the construction of 4-to-1 multiplexer. x0, x1, x2 and x3 are the inputs and C1 and C0 are the select lines and M is the output.

10. How many select lines would be required for an 8-line-to-1-line multiplexer?
a) 2
b) 4
c) 8
d) 3

Answer: d
Explanation: 2n input lines, n control lines and 1 output line available for MUX. Here, 8 input lines mean 23 inputs. So, 3 control lines are possible. Depending on the status of the select lines, the input is selected and fed to the output.

8. In a multiplexer, the selection of a particular input line is controlled by _____
a) Data controller
b) Selected lines
c) Logic gates
d) Both data controller and selected lines

Answer: b
Explanation: The selection of a particular input line is controlled by a set of selected lines in a multiplexer, which helps to select a particular input from several sources.

9. If the number of n selected input lines is equal to 2^m then it requires _____ select lines.
a) 2
b) m
c) n
d) 2n

Answer: b
Explanation: If the number of n selected input lines is equal to 2^m then it requires m select lines to select one of m select lines.

1. The word demultiplex means _____
a) One into many
b) Many into one
c) Distributor
d) One into many as well as Distributor

Answer: d
Explanation: The word demultiplex means “one into many” and distributor. A demultiplexer sends a single input to multiple outputs, depending on the select lines. It is clear from the diagram:

1. How many inputs will a decimal-to-BCD encoder have?
a) 4
b) 8
c) 10
d) 16

Answer: c
Explanation: An encoder is a combinational circuit encoding the information of 2n input lines to n output lines, thus producing the binary equivalent of the input. Thus, a Decimal-to-bcd converter has decimal values as inputs which range from 0-9. So, a total of 10 inputs are there in a decimal-to-BCD encoder.

2. How many outputs will a decimal-to-BCD encoder have?
a) 4
b) 8
c) 12
d) 16

Answer: a
Explanation: An encoder is a combinational circuit encoding the information of 2n input lines to n output lines, thus producing the binary equivalent of the input. Thus, a decimal to BCD encoder has 4 outputs.

5. Can an encoder be a transducer?
a) Yes
b) No
c) May or may not be
d) Both are not even related slightly

Answer: a
Explanation: Of course, a transducer is a device that has the capability to emit data as well as to accept. Transducer converts signal from one form of energy to another.

10. Can an encoder be called a multiplexer?
a) No
b) Yes
c) Sometimes
d) Never

Answer: b
Explanation: A multiplexer or MUX is a combination circuit that contains more than one input line, one output line and more than one selection line. Whereas, an encoder is also considered a type of multiplexer but without a single output line and without any selection lines.

1. A latch is an example of a _____
a) Monostable multivibrator
b) Astable multivibrator
c) Bistable multivibrator
d) 555 timer

Answer: c

2. Latch is a device with _____
a) One stable state
b) Two stable state
c) Three stable state
d) Infinite stable states

Answer: b
Explanation: Since a latch works on the principal of bistable multivibrator. A Bistable multivibrator is one in which the circuit is stable in either of two states. It can be flipped from one state to the other state and vice-versa. So a latch has two stable states.

3. Why latches are called memory devices?
a) It has capability to stare 8 bits of data
b) It has internal memory of 4 bit

c) It can store one bit of data
d) It can store infinite amount of data

Answer: c
Explanation: Latches can be memory devices, and can store one bit of data for as long as the device is powered. Once device is turned off, the memory gets refreshed.

4. Two stable states of latches are _____
a) Astable & Monostable
b) Low input & high output
c) High output & low output
d) Low output & high input

Answer: c
Explanation: A latch has two stable states, following the principle of Bistable Multivibrator. There are two stable states of latches and these states are high-output and low-output.

5. How many types of latches are _____
a) 4
b) 3
c) 2
d) 5

Answer: a
Explanation: There are four types of latches: SR latch, D latch, JK latch and T latch. D latch is a modified form of SR latch whereas, T latch is an advanced form of JK latch.

1. In digital logic, a counter is a device which _____
a) Counts the number of outputs
b) Stores the number of times a particular event or process has occurred
c) Stores the number of times a clock pulse rises and falls
d) Counts the number of inputs

Answer: b
Explanation: In digital logic and computing, a counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal.

2. A counter circuit is usually constructed of _____
a) A number of latches connected in cascade form
b) A number of NAND gates connected in cascade form
c) A number of flip-flops connected in cascade
d) A number of NOR gates connected in cascade form

Answer: c
Explanation: A counter circuit is usually constructed of a number of flip-flops connected in cascade. Preferably, JK Flip-flops are used to construct counters and registers.

3. What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of ‘n’ number of flip-flops?
a) 0 to 2n
b) 0 to 2n + 1
c) 0 to 2n – 1
d) 0 to 2n+1/2

Answer: c
Explanation: The maximum possible range of bit-count specifically in n-bit binary counter consisting of ‘n’ number of flip-flops is 0 to 2n-1. For say, there is a 2-bit counter, then it will count till 22-1 = 3. Thus, it will count from 0 to 3.

4. How many types of the counter are there?
a) 2
b) 3
c) 4
d) 5

Answer: b
Explanation: Counters are of 3 types, namely, (i)asynchronous/synchronous, (ii)single and multi-mode & (iii)modulus counter. These further can be subdivided into Ring Counter, Johnson Counter, Cascade Counter, Up/Down Counter and such like.

5. A decimal counter has _____ states.
a) 5
b) 10
c) 15
d) 20

Answer: b
Explanation: Decimal counter is also known as 10 stage counter. So, it has 10 states. It is also known as Decade Counter counting from 0 to 9.

6. Ripple counters are also called _____
a) SSI counters
b) Asynchronous counters
c) Synchronous counters
d) VLSI counters

Answer: b
Explanation: Ripple counters are also called asynchronous counter. In Asynchronous counters, only the first flip-flop is connected to an external clock while the rest of the flip-flops have their preceding flip-flop output as clock to them.

7. Synchronous counter is a type of _____
a) SSI counters
b) LSI counters
c) MSI counters
d) VLSI counters

Answer: c
Explanation: Synchronous Counter is a Medium Scale Integrated (MSI). In Synchronous Counters, the clock pulse is supplied to all the flip-flops simultaneously.

8. Three decade counter would have _____
a) 2 BCD counters
b) 3 BCD counters
c) 4 BCD counters
d) 5 BCD counters

Answer: b
Explanation: Three decade counter has 30 states and a BCD counter has 10 states. So, it would require 3 BCD counters. Thus, a three decade counter will count from 0 to 29.

9. BCD counter is also known as _____
a) Parallel counter
b) Decade counter
c) Synchronous counter
d) VLSI counter

Answer: b
Explanation: BCD counter is also known as decade counter because both have the same number of stages and both count from 0 to 9.

10. The parallel outputs of a counter circuit represent the _____
a) Parallel data word
b) Clock frequency
c) Counter modulus
d) Clock count

Answer: d
Explanation: The parallel outputs of a counter circuit represent the clock count. A counter counts the number of times an event takes place in accordance to the clock pulse.

1. How many natural states will there be in a 4-bit ripple counter?
a) 4
b) 8
c) 16
d) 32

Answer: c
Explanation: In an n-bit counter, the total number of states = 2n.
Therefore, in a 4-bit counter, the total number of states = 24 = 16 states.

2. A ripple counter's speed is limited by the propagation delay of _____
a) Each flip-flop
b) All flip-flops and gates
c) The flip-flops only with gates
d) Only circuit gates

Answer: a
Explanation: A ripple counter is something that is derived by other flip-flops. It's like a series of Flip Flops. Output of one FF becomes the input of the next. Because ripple counter is composed of FF only and no gates are there other than FF, so only propagation delay of FF will be taken into account. Propagation delay refers to the amount of time taken in producing an output when the input is altered.

3. One of the major drawbacks to the use of asynchronous counters is that _____
a) Low-frequency applications are limited because of internal propagation delays
b) High-frequency applications are limited because of internal propagation delays
c) Asynchronous counters do not have major drawbacks and are suitable for use in high- and low-frequency counting applications
d) Asynchronous counters do not have propagation delays, which limits their use in high-frequency applications

Answer: b
Explanation: One of the major drawbacks to the use of asynchronous counters is that High-frequency applications are limited because of internal propagation delays. Propagation delay refers to the amount of time taken in producing an output when the input is altered.

4. Internal propagation delay of asynchronous counter is removed by _____
a) Ripple counter
b) Ring counter

c) Modulus counter
d) Synchronous counter

Answer: d
Explanation: Propagation delay refers to the amount of time taken in producing an output when the input is altered. Internal propagation delay of asynchronous counter is removed by synchronous counter because clock input is given to each flip-flop individually in synchronous counter.

5. What happens to the parallel output word in an asynchronous binary down counter whenever a clock pulse occurs?
a) The output increases by 1
b) The output decreases by 1
c) The output word increases by 2
d) The output word decreases by 2

Answer: b
Explanation: In an asynchronous counter, there isn't any clock input. The output of 1st flip-flop is given to second flip-flop as clock input. So, in case of binary down counter the output word decreases by 1.

6. How many flip-flops are required to construct a decade counter?
a) 4
b) 8
c) 5
d) 10

Answer: a
Explanation: Number of flip-flop required is calculated by this formula: 2(n-1) <= N< = 2n. 24=16and23=8, therefore, 4 flip flops needed.

7. The terminal count of a typical modulus-10 binary counter is _____
a) 0000
b) 1010
c) 1001
d) 1111

Answer: c
Explanation: A binary counter counts or produces the equivalent binary number depending on the cycles of the clock input. Modulus-10 means count from 0 to 9. So, the terminal count is 9 (1001).

8. How many different states does a 3-bit asynchronous counter have?
a) 2

b) 4
c) 8
d) 16

Answer: c
Explanation: In a n-bit counter, the total number of states = 2n.
Therefore, in a 3-bit counter, the total number of states = 23 = 8 states.

9. A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay (tp(total)) is _____
a) 12 ms
b) 24 ns
c) 48 ns
d) 60 ns

Answer: d
Explanation: Since a counter is constructed using flip-flops, therefore, the propagation delay in the counter occurs only due to the flip-flops. Each bit has propagation delay = 12ns. So, 5 bits = 12ns * 5 = 60ns.

10. An asynchronous 4-bit binary down counter changes from count 2 to count 3. How many transitional states are required?
a) 1
b) 2
c) 8
d) 15

Answer: d
Explanation: Transitional state is given by (2n – 1). Since, it's a 4-bit counter, therefore, transition states = 24 – 1 = 15. So, total transitional states are 15.

11. A 4-bit ripple counter consists of flip-flops, which each have a propagation delay from clock to Q output of 15 ns. For the counter to recycle from 1111 to 0000, it takes a total of _____
a) 15 ns
b) 30 ns
c) 45 ns
d) 60 ns

Answer: d
Explanation: Since a counter is constructed using flip-flops, therefore, the propagation delay in the counter occurs only due to the flip-flops. One bit change is 15 ns, so 4-bit change = 15 * 4 = 60.

12. Three cascaded decade counters will divide the input frequency by _____
a) 10
b) 20
c) 100
d) 1000

Answer: d
Explanation: Decade counter has 10 states. So, three decade counters are cascaded i.e. 10*10*10=1000 states.

13. A ripple counter's speed is limited by the propagation delay of _____
a) Each flip-flop
b) All flip-flops and gates
c) The flip-flops only with gates
d) Only circuit gates

Answer: a
Explanation: A ripple counter is something that is derived by other flip-flops. Its like a series of Flip Flops. Output of one FF becomes the input of the next. Because ripple counter is composed of FF only and no gates are there other than FF, so only propagation delay of FF will be taken into account. Propagation delay refers to the amount of time taken in producing an output when the input is altered.

14. A 4-bit counter has a maximum modulus of _____
a) 3
b) 6
c) 8
d) 16

Answer: d
Explanation: In a n-bit counter, the total number of states = 2n. Therefore, in a 4-bit counter, the total number of states = 24 = 16 states.

15. A principle regarding most display decoders is that when the correct input is present, the related output will switch _____
a) HIGH
b) To high impedance
c) To an open
d) LOW

Answer: d
Explanation: A principle regarding most display decoders is that when the correct input is present, the related output will switch LOW. Since it's an active-low device.

6. The main drawback of a ripple counter is that _____
a) It has a cumulative settling time
b) It has a distributive settling time
c) It has a productive settling time
d) It has an associative settling time

Answer: a
Explanation: The main drawback of a ripple counter is that it has a cumulative settling time (i.e. another bit is transmitted just after one consequently).

8. As the number of flip flops are increased, the total propagation delay of _____
a) Ripple counter increases but that of synchronous counter remains the same
b) Both ripple and synchronous counters increase
c) Both ripple and synchronous counters remain the same
d) Ripple counter remains the same but that of synchronous counter increases

Answer: a
Explanation: In ripple counter, the clock pulses are applied to one flip-flop only. Hence, as the number of flip-flops increases the delay increases. In the synchronous counter, clock pulses to all flip-flops are applied simultaneously.

9. A reliable method for eliminating decoder spikes is the technique called _____
a) Strobing
b) Feeding
c) Wagging
d) Waving

Answer: a
Explanation: A reliable method for eliminating decoder spikes is the technique called strobing. A strobe signal validates the availability of data on consecutive parallel lines.

10. A glitch that appears on the decoded output of a ripple counter is often difficult to see on an oscilloscope because of _____
a) It is a random event
b) It occurs less frequently than the normal decoded output
c) It is very fast
d) All of the Mentioned

Answer: d
Explanation: A glitch is a transition that occurs before a signal settles to a specific value. A glitch that appears on the decoded output of a ripple counter is often difficult to see on an oscilloscope because it is a random event and very fast and it occurs less frequently than the normal decoded output.

1. A register is defined as _____
a) The group of latches for storing one bit of information
b) The group of latches for storing n-bit of information
c) The group of flip-flops suitable for storing one bit of information
d) The group of flip-flops suitable for storing binary information

Answer: d
Explanation: A register is defined as the group of flip-flops suitable for storing binary information. Each flip-flop is a binary cell capable of storing one bit of information. The data in a register can be transferred from one flip-flop to another.

2. The register is a type of _____
a) Sequential circuit
b) Combinational circuit
c) CPU
d) Latches

Answer: a
Explanation: Register's output depends on the past and present states of the inputs. The device which follows these properties is termed as a sequential circuit. Whereas, combinational circuits only depend on the present values of inputs.

3. How many types of registers are?
a) 2
b) 3
c) 4
d) 5

Answer: c
Explanation: There are 4 types of shift registers, viz., Serial-In/Serial-Out, Serial-In/Parallel-Out, Parallel-In/Serial-Out and Parallel-In/Parallel-Out.

4. The main difference between a register and a counter is _____
a) A register has no specific sequence of states
b) A counter has no specific sequence of states
c) A register has capability to store one bit of information but counter has n-bit
d) A register counts data

Answer: a
Explanation: The main difference between a register and a counter is that a register has no specific sequence of states except in certain specialised applications.

5. In D register, ‘D’ stands for _____
a) Delay
b) Decrement
c) Data
d) Decay

Answer: c
Explanation: D stands for “data” in case of flip-flops and not delay. Registers are made of a group of flip-flops.

6. Registers capable of shifting in one direction is _____
a) Universal shift register
b) Unidirectional shift register
c) Unipolar shift register
d) Unique shift register

Answer: b
Explanation: The register capable of shifting in one direction is unidirectional shift register. The register capable of shifting in both directions is known as a bidirectional shift register.

7. A register that is used to store binary information is called _____
a) Data register
b) Binary register
c) Shift register
d) D – Register

Answer: b
Explanation: A register that is used to store binary information is called a binary register. A register in which data can be shifted is called shift register.

8. A shift register is defined as _____
a) The register capable of shifting information to another register
b) The register capable of shifting information either to the right or to the left
c) The register capable of shifting information to the right only
d) The register capable of shifting information to the left only

Answer: b
Explanation: The register capable of shifting information either to the right or to the left is termed as shift register. A register in which data can be shifted only in one direction is called unidirectional shift register, while if data can shifted in both directions, it is known as a bidirectional shift register.

9. How many methods of shifting of data are available?
a) 2

b) 3
c) 4
d) 5

Answer: a
Explanation: There are two types of shifting of data are available and these are serial shifting & parallel shifting.

10. In serial shifting method, data shifting occurs _____
a) One bit at a time
b) simultaneously
c) Two bit at a time
d) Four bit at a time

Answer: a
Explanation: As the name suggests serial shifting, it means that data shifting will take place one bit at a time for each clock pulse in a serial fashion. While in parallel shifting, shifting will take place with all bits simultaneously for each clock pulse in a parallel fashion.

1. Based on how binary information is entered or shifted out, shift registers are classified into _____ categories.
a) 2
b) 3
c) 4
d) 5

Answer: c
Explanation: The registers in which data can be shifted serially or parallelly are known as shift registers. Based on how binary information is entered or shifted out, shift registers are classified into 4 categories, viz., Serial-In/Serial-Out(SISO), Serial-In/Parallel-Out (SIPO), Parallel-In/Serial-Out (PISO), Parallel-In/Parallel-Out (PIPO).

2. The full form of SIPO is _____
a) Serial-in Parallel-out
b) Parallel-in Serial-out
c) Serial-in Serial-out
d) Serial-In Peripheral-Out

Answer: a
Explanation: SIPO is always known as Serial-in Parallel-out.

3. A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as?

a) Tristate
b) End around
c) Universal
d) Conversion

Answer: c
Explanation: A shift register can shift it's data either left or right. The universal shift register is capable of shifting data left, right and parallel load capabilities.

4. How can parallel data be taken out of a shift register simultaneously?
a) Use the Q output of the first FF
b) Use the Q output of the last FF
c) Tie all of the Q outputs together
d) Use the Q output of each FF

Answer: d
Explanation: Because no other flip-flops are connected with the output Q, therefore one can use the Q out of each FF to take out parallel data.

5. What is meant by the parallel load of a shift register?
a) All FFs are preset with data
b) Each FF is loaded with data, one at a time
c) Parallel shifting of data
d) All FFs are set with data

Answer: a
Explanation: At Preset condition, outputs of flip-flops will be 1. Preset = 1 means Q = 1, thus input is definitely 1.

1. A sequence of equally spaced timing pulses may be easily generated by which type of counter circuit?
a) Ring shift
b) Clock
c) Johnson
d) Binary

Answer: a
Explanation: In Ring counter, the feedback of the output of the FF is fed to the same FF's input. Thus, it generates equally spaced timing pulses.

3. To operate correctly, starting a ring shift counter requires _____
a) Clearing all the flip-flops
b) Presetting one flip-flop and clearing all others

c) Clearing one flip-flop and presetting all others
d) Presetting all the flip-flops

Answer: b
Explanation: In Ring counter, the feedback of the output of the FF is fed to the same FF's input. To operate correctly, starting a ring shift counter requires presetting one flip-flop and clearing all others so that it can shift to the next bit.

5. How many clock pulses will be required to completely load serially a 5-bit shift register?
a) 2
b) 3
c) 4
d) 5

Answer: d
Explanation: A register is a collection of FFS. To load a bit, we require 1 clock pulse for 1 shift register. So, for 5-bit shift register we would require of 5 clock pulses.

6. How is a strobe signal used when serially loading a shift register?
a) To turn the register on and off
b) To control the number of clocks
c) To determine which output Qs are used
d) To determine the FFs that will be used

Answer: b

Explanation: A strobe is used to validate the availability of data on the data line. It (an auxiliary signal used to help synchronize the real data in an electrical bus when the bus components have no common clock) signal is used to control the number of clocks during serially loading a shift register.

8. What are the three output conditions of a three-state buffer?
a) HIGH, LOW, float
b) High-Z, 0, float
c) Negative, positive, 0
d) 1, Low-Z, float

Answer: a
Explanation: Three conditions of a three-state buffer are HIGH, LOW & float.

9. The primary purpose of a three-state buffer is usually _____
a) To provide isolation between the input device and the data bus
b) To provide the sink or source current required by any device connected to its output without loading down the output device

c) Temporary data storage
d) To control data flow

Answer: a
Explanation: The primary purpose of a three-state buffer is usually to provide isolation between the input device or peripheral devices and the data bus. Three conditions of a three-state buffer are HIGH, LOW & float.

10. What is the difference between a ring shift counter and a Johnson shift counter?
a) There is no difference
b) A ring is faster
c) The feedback is reversed
d) The Johnson is faster

Answer: c
Explanation: A ring counter is a shift register (a cascade connection of flip-flops) with the output of the last one connected to the input of the first, that is, in a ring. Whereas, a Johnson counter (or switchtail ring counter, twisted-ring counter, walking-ring counter, or Moebius counter) is a modified ring counter, where the output from the last stage is inverted and fed back as input to the first stage.

Operator	Description
&	bitwise AND
|	bitwise OR
^	bitwise exclusive OR
<<	shift left
>>	shift right
~	one's complement

1. The & (bitwise AND) in C takes two numbers as operands and does AND on every bit of two numbers. The result of AND is 1 only if both bits are 1.
2. The | (bitwise OR) in C takes two numbers as operands and does OR on every bit of two numbers. The result of OR is 1 if any of the two bits is 1.
3. The ^ (bitwise XOR) in C takes two numbers as operands and does XOR on every bit of two numbers. The result of XOR is 1 if the two bits are different.
4. The << (left shift) in C takes two numbers, the left shifts the bits of the first operand, and the second operand decides the number of places to shift.
5. The >> (right shift) in C takes two numbers, right shifts the bits of the first operand, and the second operand decides the number of places to shift.
6. The ~ (bitwise NOT) in C takes one number and inverts all bits of it.

2. Which of the following is correct about 8086 microprocessor?
a) Intel's first x86 processor
b) Motrola's first x86 processor
c) STMICROELECTRONICS's first x86 processor
d) NanoXplore x86 processor

Answer: a

Explanation: The Intel 8086 is Intel's first x86 processor. They launched the most powerful processor in terms of advanced architecture i.e. 8086 processor in 1978. It has larger memory addressing capability and a powerful instruction set.

3. Which of the following is a type of microprocessor?
a) CISC
b) RISC
c) EPIC
d) All of the mentioned

Answer: d
Explanation: They are of three types:
CISC: Complex Instruction Set Computer
RISC: Reduced Instruction Set Computer
EPIC: Explicitly Parallel Instruction Computing

4. The microprocessor of a computer can operate on any information if it is present in _____ only.
a) Program Counter
b) Flag
c) Main Memory
d) Secondary Memory

Answer: c
Explanation: If the information isn't in the computer's main store, the microprocessor can't do anything with it. The primary storage area in a computer, also known as main storage or memory, is where data is stored for easy access by the computer's processor. Random-access memory (RAM) and memory are frequently used interchangeably to refer to primary or main storage.

5. Which of the following technology was used by Intel to design its first 8-bit microprocessor?
a) NMOS
b) HMOS
c) PMOS
d) TTL

Answer: a
Explanation: NMOS was used in 8080 microprocessors whereas HMOS was used in 8085 microprocessors.

6. Which of the following addressing method does the instruction, MOV AX,[BX] represent?
a) register indirect addressing mode
b) direct addressing mode
c) register addressing mode
d) register relative addressing mode

Answer: a
Explanation: In register indirect addressing mode the address of the operand is stored in the register. Since the instruction specifies that the register used to refer to the address is accessed indirectly, it represents the register indirect addressing mode.

7. What is the word length of an 8-bit microprocessor?
a) 8-bits – 64 bits
b) 4-bits – 32 bits
c) 8-bits – 16 bits
d) 8-bits – 32 bits

Answer: a
Explanation: At a time, an 8-bit CPU can process 8 bits of data. Depending on the type of microcomputer, the word length might range from 4 to 64 bits.

8. In 8-bit microprocessor, how many opcodes are present?
a) 246
b) 278
c) 250
d) 256

Answer: a
Explanation: In an 8-bit microprocessor, maximum 28 = 256 opcodes are possible. But it consists of only 246 opcodes.

9. Which of the following is not true about the address bus?
a) It consists of control PIN 21 to 28
b) It is a bidirectional bus
c) It is 16 bits in length
d) Lower address bus lines (AD0 – AD7) are called “Line number”

Answer: b
Explanation: Data bus in the microprocessor is bidirectional but the address bus is unidirectional. AD0 – AD7 are the address lines that can be used for both address and data bus lines.

10. Which of the following is true about microprocessors?
a) It has an internal memory
b) It has interfacing circuits
c) It contains ALU, CU, and registers
d) It uses Harvard architecture

Answer: c
Explanation: Microprocessors don't have memory and interfacing circuits. They follow Princeton architecture and they contain ALU, CU, and registers inside them.

11. Which of the following is the correct sequence of operations in a microprocessor?
a) Opcode fetch, memory read, memory write, I/O read, I/O write
b) Opcode fetch, memory write, memory read, I/O read, I/O write
c) I/O read, opcode fetch, memory read, memory write, I/O write
d) I/O read, opcode fetch, memory write, memory read, I/O write

Answer: a
Explanation: Initially, the opcode is fetched from memory, then memory read and write operations are performed followed by I/O read and I/O write operations.

12. The _____ directive instructs the assembler to begin memory allocation for a segment/block/code from the stated address.
a) GROUP
b) OFFSET
c) ORG
d) LABEL

Answer: c
Explanation: When an ORG is written, the assembler starts the location counter to keep track of the module's allotted address as specified in the directive.
The location counter is initialized to 0000H if the directive is not present.

13. Which of the following is not a microprocessor?
a) Z8000
b) Motorola 6809
c) Zilog Z8
d) PIC1x

Answer: d
Explanation: Z8000, Motorola 6809, and Zilog Z8 are microprocessors but PIC1x is an 8-bit microcontroller.

14. Which of the following is not a property of TRAP interrupt in microprocessor?
a) It is a non-maskable interrupt
b) It is of highest priority
c) It uses edge-triggered signal
d)It is a vectored interrupt

Answer: c
Explanation: TRAP interrupt in 8085 microprocessor uses both level and edge-triggered clock because it is of highest priority among all the interrupts.

15. Which of the following is a property of RST 7.5 interrupt?
a) It is a non-maskable interrupt
b) It has 3rd highest priority
c) It uses level-triggered signal
d) Its vectored address is 003C H

Answer: d
Explanation: RST 7.5 is a maskable interrupt with 2nd highest priority after RST-4.5. It uses only the edge-triggered signal. It is a vectored interrupt and its vectored address is 003C H.

16. Which of the following flag is used to mask INTR interrupt?
a) zero flag
b) auxiliary carry flag flag
c) interrupt flag
d) sign flag

Answer: c
Explanation: If the interrupt flag, IF=1, is set, the microprocessor will serve any interrupt. The processor ignores the service if the interrupt flag, IF=0, is set to 0.

17. Which of the following is a special-purpose register of microprocessor?
a) Program counter
b) Instruction register
c) Accumulator
d) Temporary register

Answer: a
Explanation: Instruction register, accumulator, and temporary register are general-purpose registers

but program counter is a special-purpose register because it holds the address of the next instruction.

18. Which of the following circuit is used as a special signal to demultiplex the address bus and data bus?
a) Priority Encoder
b) Decoder
c) Address Latch Enable
d) Demultiplexer

Answer: c
Explanation: Address Latch Enable is a positive pulse and it is generated whenever the microprocessor starts an operation to latch the lower order address lines (AD7 to AD0).

19. How many flip-flops are there in a flag register of 8085 microprocessor?
a) 4
b) 5
c) 7
d) 10

Answer: b
Explanation: There are five flags or flip-flops in a flag register in 8085 microprocessor that shows the status after ALU operation. They are mainly affected by the content of the accumulator.

20. Which of the following flag condition is used for BCD arithmetic operations in microprocessor?
a) Sign flag
b) Auxiliary carry flag
c) Parity flag
d) Zero flag

Answer: b
Explanation: Among all the five flag conditions in microprocessor, the auxiliary carry flag is used internally for BCD arithmetic operations. Based on the auxiliary flag, the instruction set doesn’t contain the conditional jump operation.

21. Whenever a non-maskable interrupt occurs in 8085 microprocessor, which of the following data line contains the data?
a) 2C H
b) 3C H
c) 36 H
d) 24 H

Answer: d
Explanation: TRAP interrupt is a non-maskable interrupt with the highest priority. When it occurs, its vectored address 0024 H is placed on the program counter. 24 H is the lower address bus which also acts as the data bus.

22. What does a microprocessor understand after decoding opcode?
a) Perform ALU operation
b) Go to memory
c) Length of the instruction and number of operations
d) Go to the output device

Answer: c
Explanation: After decoding the opcode of the instruction, a microprocessor understands the length of the instruction and the total number of operations to be performed.

23. How many address lines are present in 8086 microprocessor?
a) 16
b) 20
c) 32
d) 40

Answer: b
Explanation: 8086 microprocessor is a 16-bit microprocessor that uses 20 address lines and 16 data lines. AD0 to AD15 are 16 lower order address lines that can be operated in both address and data bus mode.

24. Which of the following is not a status flag in microprocessor?
a) Overflow flag
b) Direction flag
c) Interrupt flag
d) Index flag

Answer: d
Explanation: Overflow flag represents whether the result is out of scope or not. Direction flag is used in string operations and interrupt flag is used to enable the interrupts.

25. Which of the following is not a condition flag?
a) Trap flag
b) Auxiliary carry flag
c) Parity flag
d) Zero flag

Answer: a
Explanation: Trap, direction, and interrupt are the control flags. Carry, parity, auxiliary carry, zero, sign and overflow flags are the condition flags.

26. Which of the following register is not used in opcode fetch operations?
a) Program counter
b) Memory address register
c) Memory data register
d) Flag register

Answer: d
Explanation: Flag register is not used in opcode fetch operations. It is used to represent the status of ALU operation which is performed after decoding of the opcode.

27. A memory connected to a microprocessor has 20 address lines and 16 data lines. What will be the memory capacity?
a) 8 KB
b) 2 MB
c) 16 MB
d) 64 KB

Answer: b
Explanation: Total number of locations of the memory possible for 20 address lines is 220 and every location has 16/8 = 2 bytes. So, total memory capacity will be 220 × 2 = 2 MB.

28. What is the word length of the Pentium-II microprocessor?
a) 8-bit
b) 32-bit
c) 64-bit
d) 16-bit

Answer: c
Explanation: The Pentium-II microprocessor is a 64-bit microprocessor. It was introduced in 1997 and designed with 7.5 million transistors. Its word length is 64-bit.

29. Which of the following is not true about 8085 microprocessor?
a) It is an 8-bit microprocessor
b) It is a 40 pin DIP chip
c) It is manufactured using PMOS technology
d) It has 16 address lines

Answer: c
Explanation: 8085 microprocessor is manufactured using NMOS technology. PMOS technology is used in a 4004 microprocessors. NMOS technology is faster than PMOS technology.

30. Which of the following is a non-vectored input?
a) TRAP
b) RST-7.5
c) RST-6.5
d) INTR

Answer: d
Explanation: TRAP, RST-7.5, and RST-6.5 are vectored inputs but INTR is a non-vectored input. It has the least priority and its address is provided by the user using an external device.

31. Which of the following is true?
a) Every instruction has two parts i.e. opcode and operands
b) MOV B, C is a two-byte instruction
c) MVI A, 90H is a three-byte instruction
d) Maximum number of T-states possible for the execution of an instruction is 16

Answer: a
Explanation: MOV B, C is a one-byte instruction. MVI A, 90H is a two-byte instruction and the maximum number of T-states possible for the execution of an instruction in 8085 microprocessor is 18.

32. Which of the following addressing mode is used by 8085 microprocessor for array and list operations?
a) Base-Register
b) Direst
c) Indexed
d) Immediate

Answer: c
Explanation: Indexed addressing mode is used for array and list operations. It uses a constant value and index register to execute the instruction.

33. What is stored in the H & L general-purpose register?
a) Opcode
b) Address of memory
c) Address of next instruction
d) Temporary data

Answer: b
Explanation: H and L are 8-bit general-purpose registers. They are used to store the address of memory. Together they can store a 16-bit address.

34. If a 90 GB memory has to be connected to a microprocessor, minimum how many address lines are required?
a) 36
b) 39
c) 32
d) 37

Answer: d
Explanation: 90 GB is greater than 64 GB and less than 128 GB. For 64 GB (236 Bytes), a minimum of 36 address lines are needed. So, for 90 GB, we need 36 + 1 = 37 address lines.

35. Which of the following is a software interrupt?
a) TRAP
b) INTR
c) RST-6.5
d) RST-5

Answer: d
Explanation: TRAP, INTR, and RST-6.5 are the hardware interrupts but RST-5 is a software interrupt present. All software interrupts are vectored interrupts.

36. What is the vectored address of RST-5?
a) 0010 H
b) 0032 H
c) 0028 H
d) 0030 H

Answer: c
Explanation: Vectored address of RST-n is calculated by the formula n × 8. So, vectored address of RST-5 is (40)10. (40)10 in hexadecimal is (28)16 = 0028 H.

37. Which of the following is true about stack pointer?
a) Stack pointer contains the address of the top of the stack memory
b) Stack pointer is an 8-bit register
c) Stack pointer stores data permanently
d) Stack pointer is initialized after stack operation

Answer: a
Explanation: Stack pointer is initialized before stack operation, it is a 16-bit register that stores data temporarily. It follows a LIFO operation. So, it contains the address of the top of the stack memory.

38. How many address lines are required to connect a 4 KB RAM to a microprocessor?
a) 10
b) 16
c) 12
d) 20

Answer: c
Explanation: 4 KB RAM is equal to 4096 × 8 bits. Total number locations are (4096 × 8)/8 = 4096 and 4096 = 212. So, 12 address lines are required to connect a 4 KB RAM to a microprocessor.

39. Which of the following is true about MOV A, B instruction?
a) It means move the content of register A to register B
b) It uses immediate addressing mode
c) It doesn't affect the flag register
d) It is a 2-byte instruction

Answer: c
Explanation: MOV A, B means moving the content of register B to register A. It is a 1-byte instruction and it uses register addressing mode. No flags are affected because operations of this instruction are not performed in the ALU.

40. Which of the following is false about LDA instruction?
a) It is a 3-byte instruction
b) It uses indirect addressing mode
c) It has 13 T-states
d) It doesn't affect any flags

Answer: b
Explanation: LDA is a direct addressing mode instruction which stands for Load Accumulator Direct. It is a 3-byte instruction and it has 13 T-states. No flags are affected by this instruction.

41. Which is of the following is true about STA instruction?
a) It uses immediate addressing mode
b) It is a 3-byte instruction
c) It required three machine cycles
d) Accumulator is loaded with the content of memory

Answer: b
Explanation: STA is a direct addressing mode instruction which stands for Store Accumulator Direct.

It is a 3-byte instruction and it requires four machine cycles. In STA instruction memory is loaded with the content of the accumulator.

42. DAA instruction is used to perform which type of addition?
a) BCD addition
b) Excess-3 addition
c) Binary addition
d) Octal addition

Answer: a
Explanation: DAA instruction is used to perform BCD addition. DAA instruction changes the binary values of the contents of the accumulator to BCD.

43. What does a loader do in a microprocessor?
a) Converts hexadecimal code to binary
b) Converts decimal to binary
c) Increments the content of the program counter by 1
d) Decodes an opcode

Answer: a
Explanation: Microprocessor understands only 0s & 1s. So, a loader first converts hexadecimal code to binary form and then loads it to the memory.

44. Suppose registers ‘A’ and ‘B’ contain 50H and 40H respectively. After instruction MOV A, B, what will be the contents of registers A and B?
a) 40H, 40H
b) 50H, 40H
c) 50H, 50H
d) 60H, 40H

Answer: a
Explanation: Initially, register A contains 50H & B contains 40H. Instruction MOV A, B means move the content of B to A. So, after this operation, both registers A & B will contain 40H.

45. For how many times per instruction, the content of the program counter is placed on the address bus?
a) One time
b) Two times
c) Depends on the memory capacity of the processor
d) Depends on the length of the instruction

Answer: d
Explanation: After decoding an opcode the microprocessor understands the length of the instruction.

So, the content of the program counter is placed on the address bus as many times as the length of the instruction.

46. Conditional instructions are independent of which of the following flag?
a) Z
b) AC
c) CY
d) P

Answer: b
Explanation: Conditional instructions are the branching instructions. In this group, the program control is transferred from one location to another conditionally. They depend on the status of flags affected for previous ALU operations accept the AC flag.

47. Which of the following is not correct about HLT instruction?
a) It is a machine control instruction
b) It is used to start the execution of the program
c) PC is disconnected from the address bus
d) A reset interrupt is required to come out of halt state

Answer: b
Explanation: HLT is a machine control statement. Internally, the PC is disconnected from the address bus so, the next fetch is not possible. It is used mainly to stop the execution of the program.

48. When data required for instruction is present inside the register of a microprocessor then which of the following addressing mode is used?
a) Indexed
b) Register
c) Relative
d) Direct

Answer: b
Explanation: Register addressing mode is used when data is present inside the register of the microprocessor. For example, MOV B, C. Here, B and C are the registers of the microprocessor.

49. Which of the following interfacing IC is a DMA controller?
a) 8257/37
b) 8155
c) 8253/54
d) 8279

Answer: a
Explanation: 8155 is a multipurpose programmable I/O device. 8253/54 is a programmable counter. 8279 is a keyboard/display controller and 8257/37 is a DMA controller.

50. Which of the following is a 2-word instruction set?
a) LDA 2500H
b) MOV A, B
c) IN 01H
d) JMP 2085H

Answer: c
Explanation: LDA 2500H and JMP 2085H are 3-word instructions. MOV A, B is a 1-word instruction. IN 01H is a 2-word instruction, the first byte specifies the opcode and the second byte specifies the operand.

51. Which of the following is a register-indirect addressing mode instruction set?
a) LDA 2700H
b) ADI 36H
c) DAA
d) LDAX B

Answer: d
Explanation: LDA 2700H is a direct addressing mode instruction. ADI 36H is an immediate addressing mode instruction. DAA is an implicit addressing mode and LDAX B is a register-indirect addressing mode instruction.

52. Which is of the following is true about SPHL instruction?
a) It uses indexed addressing mode
b) It is a 3-byte instruction
c) It requires three T-states
d) Contents of HL pair is moved to SP

Answer: d
Explanation: SPHL is a 1-byte instruction. It uses register addressing mode. It required 6 T-states and it means moving the contents of the HL pair to SP.

- **Differences between 8085 and 8086 Microprocessor**

• 8085 microprocessor	• 8086 microprocessor

• The data bus is 8 bits.	• The data bus is 16 bits.
• The address bus is 16 bits.	• The address bus is 20 bits.
• The memory capacity is 64 KB. Also, 8085 Can Perform Operation Up to 28 i.e. 256 numbers. A number greater than this is to be taken multiple times in an 8-bit data bus.	• The memory capacity is 1 MB. Also, 8086 Can Perform operations up to 216 i.e. 65,536 numbers.
• The input/output port addresses are 8 bits.	• The input/output port addresses are 16 bits.
• The operating frequency is 3.2 MHz.	• The operating frequency is 5 MHz, 8 MHz, and 10 MHz.
• 8085 MP has a Single Mode Of Operation.	• 8086 MP has Two Modes Of Operation. 1. Minimum Mode = Single CPU PROCESSOR 2. Maximum Mode = Multiple CPU PROCESSOR.
• It does not have multiplication and division instructions.	• It has multiplication and division instructions.

• It does not support pipelining.	• It supports pipe-lining as it has two independent units Execution Unit (EU) and Bus Interface Unit (BIU).
• It does not support an instruction queue.	• It supports an instruction queue.
• Memory space is not segmented.	• Memory space is segmented.
• It consists of 5 flags(Sign Flag, Zero Flag, Auxiliary Carry Flag, Parity Flag, and Carry Flag).	• It consists of 9 flags(Overflow Flag, Direction Flag, Interrupt Flag, Trap Flag, Sign Flag, Zero Flag, Auxiliary Carry Flag, Parity Flag, and Carry Flag).
• It is a low-cost Microprocessor	• It is a comparatively High-cost Microprocessor.
• There are 5 Addressing Modes.	• There are 11 addressing modes.
• There is no concurrency in Fetching, Decoding, and execution.	• There is Concurrency in Fetching, Decoding, and Execution because of the instruction queue.
• It has almost 6500 transistors.	• It has almost 29000 transistors.

• It is Accumulator based Microprocessor because Accumulator contains major activity in ALU Operations in store and updating calculations.	• It is General Purpose Registers(GPR) based microprocessor because there is no specific Accumulator attached to the input of ALU. all GPRs are connected with it via Bus.
• Integer, Decimal, and Hexadecimal arithmetic is supported	• It also supports ASCII Arithmetic over Integer, Decimal, and Hexadecimal.
• It needed less external hardware.	• It needed more external hardware. Because here more than 1 processor works and an additional external processor can also be employed as per requirements.
• It runs over 50% duty cycle. That means for one instruction cycle clock pulse held high for 50% of the pulse.	• It runs over a 33% duty cycle. That means for one instruction cycle clock pulse held high for 33% of the pulse.
• In the 8085 Microprocessor for immediate addressing modes there are instructions containing “I” in it. e.g. MVI, LXI, etc.	• In the 8086 Microprocessor for immediate addressing modes there is no instruction containing “I” in it. In other words, there is no MVI instruction in 8086 for moving/transferring data. Only MOV instruction is sufficient.

• In 8085 microprocessor ADD, SUB instructions were carried out in Accumulator by default. It used only 1 register for arithmetic operations because another register is fixed and is an accumulator. • Example: **ADD C** will do **[A]<- [A] + [C]**	• In the 8086 microprocessor, we can give the source and destination register and according to that addition or any arithmetic operations will be performed. • For Example: **ADD AX, BX** will do [**AX] <- [AX] + [BX]**
• The 8085 microprocessor operates at 5 volts.	• The 8086 microprocessor operates at 5 or 3.3 volts.
• Less powerful and faster than 8086 microprocessor	• The 8086 microprocessor is faster and more powerful than the 8085 microprocessor.
• The 8085 microprocessor handles interrupts using a software-based approach.	• The 8086 microprocessor uses a hardware-based approach.

1. The instruction, MOV AX, 0005H belongs to the address mode
a) register
b) direct
c) immediate
d) register relative

Answer: c
Explanation: In Immediate addressing mode, immediate data is a part of instruction and appears in the form of successive byte or bytes.

2. The instruction, MOV AX, 1234H is an example of
a) register addressing mode

b) direct addressing mode
c) immediate addressing mode
d) based indexed addressing mode

Answer: c
Explanation: Since immediate data is present in the instruction.

3. The instruction, MOV AX, [2500H] is an example of
a) immediate addressing mode
b) direct addressing mode
c) indirect addressing mode
d) register addressing mode

Answer: b
Explanation: Since the address is directly specified in the instruction as a part of it.

4. If the data is present in a register and it is referred using the particular register, then it is
a) direct addressing mode
b) register addressing mode
c) indexed addressing mode
d) immediate addressing mode

Answer: b
Explanation: Since register is used to refer the address.

5. The instruction, MOV AX,[BX] is an example of
a) direct addressing mode
b) register addressing mode
c) register relative addressing mode
d) register indirect addressing mode

Answer: d
Explanation: Since the register used to refer to the address is accessed indirectly.

6. If the offset of the operand is stored in one of the index registers, then it is
a) based indexed addressing mode
b) relative based indexed addressing mode
c) indexed addressing mode
d) none of the mentioned

Answer: c
Explanation: In the indexed addressing mode, the offset of an operand is stored and in the rest of them, address is stored.

7. The addressing mode that is used in unconditional branch instructions is
a) intrasegment direct addressing mode
b) intrasegment indirect addressing mode
c) intrasegment direct and indirect addressing mode
d) intersegment direct addressing mode

Answer: b
Explanation: In intrasegment indirect mode, the branch address is found as the content of a register or a memory location.

8. If the location to which the control is to be transferred lies in a different segment other than the current one, then the mode is called
a) intrasegment mode
b) intersegment direct mode
c) intersegment indirect mode
d) intersegment direct and indirect mode

Answer: d
Explanation: In intersegment mode, the control to be transferred lies in a different segment.

9. The instruction, JMP 5000H:2000H;
is an example of
a) intrasegment direct mode
b) intrasegment indirect mode
c) intersegment direct mode
d) intersegment indirect mode

Answer: c
Explanation: Since in intersegment direct mode, the address to which the control is to be transferred is in a different segment.

10. The contents of a base register are added to the contents of index register in
a) indexed addressing mode
b) based indexed addressing mode
c) relative based indexed addressing mode
d) based indexed and relative based indexed addressing mode

Answer: d
Explanation: The effective address is formed by adding the contents of both base and index registers to a default segment.

2. Which of the following is not a data copy/transfer instruction?
a) MOV
b) PUSH
c) DAS
d) POP

Answer: c
Explanation: DAS (Decimal Adjust after Subtraction) is an arithmetic instruction.

12. The expansion of DAA is
a) decimal adjust after addition
b) decimal adjust before addition
c) decimal adjust accumulator
d) decimal adjust auxiliary

Answer: c
Explanation: This instruction performs conversion operation.

13. The instruction that is used to convert the result of the addition of two packed BCD numbers to a valid BCD number is
a) DAA
b) DAS
c) AAA
d) AAS

Answer: a
Explanation: In this conversion, the result has to be only in AL.

8. The instruction that unconditionally transfers the control of execution to the specified address is
a) CALL
b) JMP
c) RET
d) IRET

Answer: b
Explanation: In this the control transfers to the address specified in the instruction and flags are not affected by this instruction.

9. Which instruction cannot force the 8086 processor out of ‘halt’ state?
a) Interrupt request
b) Reset
c) Both interrupt request and reset
d) Hold

Answer: d
Explanation: Only an interrupt request or Reset will force the 8086 processor to come out of the ‘halt’ state.

10. NOP instruction introduces
a) Address
b) Delay
c) Memory location
d) None of the mentioned

Answer: b
Explanation: NOP is the No operation. It means that the processor performs no operation for the clock cycle and thus there exists a delay.

11. Which of the following is not a machine controlled instruction?
a) HLT
b) CLC
c) LOCK
d) ESC

Answer: b
Explanation: Since CLC is a flag manipulation instruction where CLC stands for Clear Carry Flag.

In the 8085 microprocessor, interrupt is a process in which control of the program transfers from the main program to the starting location defined by interrupt. It is a process by which some external device or peripheral informs microprocessor to become ready for data communication by accepting the made request. Hence, it is a signal that temporarily suspends the normal execution of a program and redirects the control to a specific interrupt service routine (ISR). Interrupts allow the microprocessor to respond to external events, such as user input, system events, or hardware signals without the need for constant polling.

Types of Interrupt Signals in the 8085 Microprocessor

There are five interrupt signals in the 8085 microprocessor:

1. **TRAP:** The TRAP interrupt is a non-maskable interrupt that is generated by an external device, such as a power failure or a hardware malfunction. The TRAP interrupt has the highest priority and cannot be disabled.
2. **RST 7.5:** The RST 7.5 interrupt is a maskable interrupt that is generated by a software instruction. It has the second highest priority.
3. **RST 6.5:** The RST 6.5 interrupt is a maskable interrupt that is generated by a software instruction. It has the third highest priority.
4. **RST 5.5:** The RST 5.5 interrupt is a maskable interrupt that is generated by a software instruction. It has the fourth highest priority.
5. **INTR:** The INTR interrupt is a maskable interrupt that is generated by an external device, such as a keyboard or a mouse. It has the lowest priority and can be disabled.

8 vector address, RST 0…..RST 7

ALU

1. The ‘heart’ of the processor which performs many different operations _____
a) Arithmetic and logic unit
b) Motherboard
c) Control Unit
d) Memory

Answer: a
Explanation: The Arithmetic and logic unit performs all the basic operations of the computer system. It performs all the arithmetic(+,-,*,/,etc) as well as the logical operations(AND, OR, NOT, etc.).

2. ALU is the place where the actual executions of instructions take place during the processing operation.
a) True
b) False

Answer: a
Explanation: ALU is a combinational electronic circuit which basically performs all the logical or the bitwise operations and the arithmetic operations. Therefore, it is the place where the actual executions of instructions take place.

3. Which of the following is not a bitwise operator?
a) |
b) ^
c) .
d) <<

Answer: c
Explanation: All except the dot(.) operator are bitwise operators.
| : Bitwise OR
^ : Bitwise XOR
<< : Shift Left

4. The sign magnitude representation of -1 is _____
a) 0001
b) 1110
c) 1000
d) 1001

Answer: d
Explanation: The first leftmost bit i.e. the most significant bit in the sign magnitude represents if the number is positive or negative. If the MSB is 1, the number is negative else if it is 0, the number is positive. Here, +1=0001 and for -1=1001.

5. IEEE stands for _____
a) Instantaneous Electrical Engineering
b) Institute of Emerging Electrical Engineers
c) Institute of Emerging Electronic Engineers
d) Institute of Electrical and electronics engineers

Answer: d
Explanation: The IEEE is an organization of professionals in the field of electronics and electrical engineering. IEEE has given certain standards of its own which are followed in the field of computer science and electrical engineering.

6. The ALU gives the output of the operations and the output is stored in the _____
a) Memory Devices
b) Registers
c) Flags
d) Output Unit

Answer: b
Explanation: Any output generated by the ALU gets stored in the registers. The registers are the temporary memory locations within the processor that are connected by signal paths to the CPU.

7. The process of division on memory spaces is called _____
a) Paging
b) Segmentation
c) Bifurcation
d) Dynamic Division

Answer: b
Explanation: The memory space is divided into segments of dynamic size. The programmer is aware of the segmentation and can reallocate the segments accordingly.

8. Number of bits in ALU is _____
a) 4
b) 8
c) 16
d) 2

Answer: c
Explanation: Arithmetic and Logic Unit consists of 16bits. They perform certain Arithmetic and bitwise operations (add, subtract, AND, OR, XOR, Increment, decrement, shift).

9. Which flag indicates the number of 1 bit that results from an operation?
a) Zero
b) Parity
c) Auxiliary
d) Carry

Answer: b
Explanation: The parity flag indicates the number of 1 bit in any operation. The resultant bit is called the parity bit. The main aim of the parity bit is to check for errors.

10. The bitwise complement of 0 is _____
a) 00000001
b) 10000000
c) 11111111
d) 11111110

Answer: c
Explanation: Bitwise complement is basically used to convert all the 0 digits to 1 and the 1s to 0s. So, for 0 = 00000000(in 8-bits) ::: 11111111(1s complement). The bitwise complement is often referred to as the 1s complement.

Computer Organization

1. What is computer architecture?
a) set of categories and methods that specify the functioning, organisation, and implementation of computer systems
b) set of principles and methods that specify the functioning, organisation, and implementation of computer systems
c) set of functions and methods that specify the functioning, organisation, and implementation of computer systems
d) None of the mentioned

Answer: b
Explanation: A set of principles and methods that specify the functioning, organisation, and implementation of computer systems is known as computer architecture. A system's architecture refers to its structure in terms of the system's individually specified components and their interrelationships.

2. What is computer organization?
a) structure and behaviour of a computer system as observed by the user
b) structure of a computer system as observed by the developer
c) structure and behaviour of a computer system as observed by the developer
d) All of the mentioned

Answer: a
Explanation: The structure and behaviour of a computer system as observed by the user is the subject of computer organisation.

3. Which of the following is a type of computer architecture?
a) Microarchitecture
b) Harvard Architecture
c) Von-Neumann Architecture
d) All of the mentioned

Answer: d
Explanation: Below are the types of Computer Architecture:
i) Von-Neumann Architecture
ii) Harvard Architecture
iii) Instruction Set Architecture
iv) Microarchitecture
v) System Design

4. Which of the following is a type of architecture used in the computers nowadays?
a) Microarchitecture
b) Harvard Architecture
c) Von-Neumann Architecture
d) System Design

Answer: c
Explanation: John von Neumann proposed this architecture. The architecture of today's computers is based on von Neumann architecture. It is based on a few ideas.

5. Which of the following is the subcategories of computer architecture?
a) Microarchitecture
b) Instruction set architecture
c) Systems design
d) All of the mentione

Answer: d
Explanation: The three main subcategories of computer architecture are:
i) Microarchitecture
ii) Instruction set architecture
iii) Systems design

6. Which of the architecture is power efficient?
a) RISC
b) ISA
c) IANA
d) CISC

Answer: a
Explanation: Hence the RISC architecture is followed in the design of mobile devices.

7. What does CSA stands for?
a) Computer Service Architecture
b) Computer Speed Addition
c) Carry Save Addition
d) None of the mentioned

Answer: b
Explanation: The CSA is used to speed up the addition of multiplicands.

8. If an exception is raised and the succeeding instructions are executed completely, then the processor is said to have _____
a) Generation word
b) Exception handling
c) Imprecise exceptions
d) None of the mentioned

Answer: c
Explanation: The processor since as executed the following instructions even though an exception was raised, hence the exception is treated as imprecise.

9. To reduce the memory access time we generally make use of _____
a) SDRAM's
b) Heaps
c) Cache's
d) Higher capacity RAM's

Answer: c
Explanation: The time required to access a part of the memory for data retrieval.

10. The IA-32 system follows which of the following design?
a) CISC
b) SIMD
c) RISC
d) None of the mentioned

Answer: a
Explanation: This system architecture is used to reduce the steps involved in execution by performing complex operations in one step.

11. Which of the following architecture is suitable for a wide range of data types?
a) IA-32
b) ARM
c) ASUS firebird
d) 68000

Answer: a
Explanation: IA-32 architecture is suitable for a wide range of data types.

12. In IA-32 architecture along with the general flags, which of the following conditional flags are provided?
a) TF
b) IOPL
c) IF
d) All of the mentioned

Answer: d
Explanation: These flags are basically used to check the system for exceptions.

13. The VLIW architecture follows _____ approach to achieve parallelism.
a) SISD
b) MIMD
c) MISD
d) SIMD

Answer: b
Explanation: The MIMD stands for Multiple Instructions Multiple Data.

14. What does VLIW stands for?
a) Very Long Instruction Width
b) Very Large Instruction Word
c) Very Long Instruction Width
d) Very Long Instruction Word

Answer: d
Explanation: It is the architecture designed to perform multiple operations in parallel.

15. In CISC architecture most of the complex instructions are stored in _____
a) CMOS
b) Register
c) Transistors
d) Diodes

Answer: c
Explanation: In CISC architecture more emphasis is given on the instruction set and the instructions take over a cycle to complete.

16. Both the CISC and RISC architectures have been developed to reduce the _____
a) Time delay
b) Semantic gap
c) Cost
d) All of the mentioned

Answer: b
Explanation: The semantic gap is the gap between the high level language and the low level language.

17. _____ are the different type/s of generating control signals.
a) Hardwired
b) Micro-instruction
c) Micro-programmed
d) Both Micro-programmed and Hardwired

Answer: d
Explanation: The above is used to generate control signals in different types of system architectures.

18. If the instruction Add R1, R2, R3 is executed in a system which is pipelined, then the value of S is (Where S is term of the Basic performance equation).
a) 2
b) ~1
c) ~7
d) 2

Answer: b
Explanation: The value will be much lower in case of multiple BUS organisation.

19. The small extremely fast, RAM's all called as _____
a) Heaps
b) Accumulators
c) Stacks
d) Cache

Answer: d
Explanation: Cache's are extremely essential in single BUS organisation to achieve fast operation.

20. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution?
a) ANSA
b) Super-scalar
c) ISA
d) All of the mentioned

Answer: b
Explanation: In super-scalar architecture, the instructions are set in groups and they're decoded and executed together reducing the amount of time required to process them.

21. What is the full form of ISA?
a) Industry Standard Architecture
b) International Standard Architecture
c) International American Standard
d) None of the mentioned

Answer: c
Explanation: The ISA is an architectural standard developed by IBM for its PC's.

22. Which of the following is the fullform of CISC?
a) Complex Instruction Sequential Compilation
b) Complete Instruction Sequential Compilation
c) Computer Integrated Sequential Compiler
d) Complex Instruction Set Computer

Answer: d
Explanation: The CISC machines are well adept at handling multiple BUS organisation.

23. The reason for the cells to lose their state over time is _____
a) Use of Shift registers
b) The lower voltage levels
c) Usage of capacitors to store the charge
d) None of the mentioned

Answer: c
Explanation: Since capacitors are used the charge dissipates over time.

24. In order to read multiple bytes of a row at the same time, we make use of _____
a) Memory extension
b) Cache
c) Shift register
d) Latch

Answer: d
Explanation: The latch makes it easy to ready multiple bytes of data of the same row simultaneously by just giving the consecutive column address.

25. The difference in the address and data connection between DRAM's and SDRAM's is _____
a) The requirement of more address lines in SDRAM's
b) The usage of a buffer in SDRAM's
c) The usage of more number of pins in SDRAM's
d) None of the mentioned

Answer: b
Explanation: The SDRAM uses buffered storage of address and data.

26. The chip can be disabled or cut off from an external connection using _____
a) ACPT
b) RESET
c) LOCK
d) Chip select

Answer: d
Explanation: The chip gets enabled if the CS is set otherwise the chip gets disabled.

27. The controller multiplexes the addresses after getting the _____ signal.
a) INTR
b) ACK
c) RESET
d) Request

Answer: d
Explanation: The controller gets the request from the device needing the memory read or write operation and then it multiplexes the address.

28. The data is transferred over the RAMBUS as _____
a) Blocks
b) Swing voltages
c) Bits
d) Packets

Answer: b
Explanation: By using voltage swings to transfer data, the transfer rate along with efficiency is improved.

29. The memory devices which are similar to EEPROM but differ in the cost effectiveness is _____
a) CMOS
b) Memory sticks
c) Blue-ray devices
d) Flash memory

Answer: d
Explanation: The flash memory functions similar to the EEPROM but is much cheaper.

30. The flash memory modules designed to replace the functioning of a hard disk is _____
a) RIMM
b) FIMM
c) Flash drives
d) DIMM

Answer: c
Explanation: The flash drives have been developed to provide faster operation but with lesser space.

31. The drawback of building a large memory with DRAM is _____
a) The Slow speed of operation
b) The large cost factor
c) The inefficient memory organisation
d) All of the mentioned

Answer: a
Explanation: The DRAM's were used for large memory modules for a long time until a substitute was found.

32. In a 4K-bit chip organisation has a total of 19 external connections, then it has _____ address if 8 data lines are there.
a) 10
b) 12
c) 9
d) 8

Answer: c
Explanation: To have 8 data lines and 19 external connections it has to have 9 address lines(i.e 4K = 512 x 8 organisation).

33. What does ISO stands for?
a) International Software Organisation
b) Industrial Software Organisation
c) International Standards Organisation
d) Industrial Standards Organisation

Answer: c
Explanation: The ISO is yet another architectural standard, used to design systems.

34. The bit used to signify that the cache location is updated is _____
a) Flag bit
b) Reference bit
c) Update bit
d) Dirty bit

Answer: d
Explanation: When the cache location is updated in order to signal to the processor this bit is used.

35. During a write operation if the required block is not present in the cache then _____ occurs.
a) Write miss
b) Write latency

c) Write hit
d) Write delay

Answer: a
Explanation: This indicates that the operation has missed and it brings the required block into the cache.

36. While using the direct mapping technique, in a 16 bit system the higher order 5 bits are used for _____
a) Id
b) Word
c) Tag
d) Block

Answer: c
Explanation: The tag is used to identify the block mapped onto one particular cache block.

37. The bit used to indicate whether the block was recently used or not is _____
a) Reference bit
b) Dirty bit
c) Control bit
d) Idol bit

Answer: b
Explanation: The dirty bit is used to show that the block was recently modified and for a replacement algorithm.

38. The number successful accesses to memory stated as a fraction is called as _____
a) Access rate
b) Success rate
c) Hit rate
d) Miss rate

Answer: c
Explanation: The hit rate is an important factor in performance measurement.

System Architecture

1. The stage in which the CPU fetches the instructions from the instruction cache in superscalar organization is
a) Prefetch stage
b) D1 (first decode) stage

c) D2 (second decode) stage
d) Final stage

Answer: a
Explanation: In the prefetch stage of pipeline, the CPU fetches the instructions from the instruction cache, which stores the instructions to be executed. In this stage, CPU also aligns the codes appropriately.

2. The CPU decodes the instructions and generates control words in
a) Prefetch stage
b) D1 (first decode) stage
c) D2 (second decode) stage
d) Final stage

Answer: b
Explanation: In D1 stage, the CPU decodes the instructions and generates control words. For simple RISC instructions, only single control word is enough for starting the execution.

3. The fifth stage of pipeline is also known as
a) read back stage
b) read forward stage
c) write back stage
d) none of the mentioned

Answer: c
Explanation: The fifth stage or final stage of pipeline is also known as “Write back (WB) stage”.

4. In the execution stage the function performed is
a) CPU accesses data cache
b) executes arithmetic/logic computations
c) executes floating point operations in execution unit
d) all of the mentioned

Answer: d
Explanation: In the execution stage, known as E-stage, the CPU accesses data cache, executes arithmetic/logic computations, and floating point operations in execution unit.

5. The stage in which the CPU generates an address for data memory references in this stage is
a) prefetch stage
b) D1 (first decode) stage
c) D2 (second decode) stage
d) execution stage

Answer: c
Explanation: In the D2 (second decode) stage, CPU generates an address for data memory references in this stage. This stage is required where the control word from D1 stage is again decoded for final execution.

6. The feature of separated caches is
a) supports the superscalar organization
b) high bandwidth
c) low hit ratio
d) all of the mentioned

Answer: d
Explanation: The separated caches have low hit ratio compared to a unified cache, but have the advantage of supporting the superscalar organization and high bandwidth.

7. In the operand fetch stage, the FPU (Floating Point Unit) fetches the operands from
a) floating point unit
b) instruction cache
c) floating point register file or data cache
d) floating point register file or instruction cache

Answer: c
Explanation: In the operand fetch stage, the FPU (Floating Point Unit) fetches the operands from either floating point register file or data cache.

8. The FPU (Floating Point Unit) writes the results to the floating point register file in
a) X1 execution state
b) X2 execution state
c) write back stage
d) none of the mentioned

Answer: c
Explanation: In the two execution stages of X1 and X2, the floating point unit reads the data from the data cache and executes the floating point computation. In the “write back stage” of pipeline, the FPU (Floating Point Unit) writes the results to the floating point register file.

9. The floating point multiplier segment performs floating point multiplication in
a) single precision
b) double precision
c) extended precision
d) all of the mentioned

Answer: d

Explanation: The floating point multiplier segment performs floating point multiplication in single precision, double precision and extended precision.

10. The instruction or segment that executes the floating point square root instructions is
a) floating point square root segment
b) floating point division and square root segment
c) floating point divider segment
d) none of the mentioned

Answer: c
Explanation: The floating point divider segment executes the floating point division and square root instructions.

11. The floating point rounder segment performs rounding off operation at
a) after write back stage
b) before write back stage
c) before arithmetic operations
d) none of the mentioned

Answer: b
Explanation: The results of floating point addition or division process may be required to be rounded off, before write back stage to the floating point registers.

12. Which of the following is a floating point exception that is generated in case of integer arithmetic?
a) divide by zero
b) overflow
c) denormal operand
d) all of the mentioned

Answer: d
Explanation: In the case of integer arithmetic, the possible floating point exceptions in Pentium are:
1. divide by zero
2. Overflow
3. denormal operand
4. Underflow
5. invalid operation.

13. The mechanism that determines whether a floating point operation will be executed without creating any exception is
a) Multiple Instruction Issue
b) Multiple Exception Issue
c) Safe Instruction Recognition
d) Safe Exception Recognition

Answer: c
Explanation: A mechanism known as Safe Exception Recognition (SER) had been employed in Pentium which determines whether a floating point operation will be executed without creating any exception.

7. Which is the simplest method of implementing hardwired control unit?
a) State Table Method
b) Delay Element Method
c) Sequence Counter Method
d) Using Circuits

Answer: a
Explanation: There are 3 ways of implementing hardwired control unit:
A state table is the simplest method in which a number of circuits are designed based on the cells in the table.
A delay element method consists of a flowchart drawn for the circuit. A D-flip flop is used as a delay element.
A sequence counter method used k-modulo counter as a replacement for k delay elements.

—-
The function of control unit in a digital computer is? to initiate sequences of micro-operations
—-

4.In general, control memory can be?
(a) ROM
(b) RAM
(c) Both A & B
(d) None

Answer: Option (a)

5.Sequencer is another name of?
(a) Control address register
(b) Control data register
(c) Next address generator
(d) Control memory

Answer: Option (c)

6.Which block holds the present microinstruction while the next address is computed and read from memory?

(a) Control address register
(b) Control data register
(c) Next address generator
(d) Control memory

Answer: Option (b)

7.In Microprogrammed control, the data register is sometimes called?
(a) Accumulator
(b) Branch register
(c) Sequence register
(d) Pipeline register

Answer: Option (d)

8.Microinstructions are stored in control memory in groups, with each group specifyin:.
(a) microprogram
(b) mapping
(c) routine
(d) none

Answer: Option (c)

9.The transformation from the instruction code bits to an address in control memory where the routine is located is referred to as _____.
(a) mapping
(b) routine
(c) scaling
(d) converting

Answer: Option (a)

10. Which of the following is not address sequencing capability?
(a) Incrementing of CAR
(b) Microinstruction in data register
(c) Branch depending on status bits
(d) Facility for subroutine call and return

Answer: Option (a)

11.Full-form of CAR?
(a) Central Address Register
(b) Central Accumulator Register
(c) Control Address Register
(d) Control Accumulator Register

Answer: Option (c)

12.The mapping function is sometimes implemented by means of an integrated circuit called _____.
(a) CAR
(b) SBR
(c) ROM
(d) PLD

Answer: Option (d)

13.Which is the best way to structure a register file that stores addresses for subroutines?
(a) FIFO
(b) LIFO
(c) FILO
(d) LILO

Answer: Option (b)

14.Full-form of SBR?
(a) Subroutine register
(b) Sub Base Register
(c) Sub Address Register
(d) None of above

Answer: Option (a)

15.How many bits microinstruction format is used in control memory?
(a) 10
(b) 12
(c) 16
(d) 20

Answer: Option (d)

16.The 20 bits of the microinstructions are divided into how many functional parts?
(a) 2
(b) 3
(c) 4
(d) 5

Answer: Option (c)

17.Which of the following is not part of microinstruction code format?
(a) SB
(b) BR
(c) CD
(d) AD

Answer: Option (a)

18.Microoperation field of microinstruction code format consists of how many bits?
(a) 1
(b) 2
(c) 3
(d) 4

Answer: Option (c)

19.CD field of microinstruction code format consists of how many bits?
(a) 5
(b) 2
(c) 3
(d) 7

Answer: Option (b)

20.BR field of microinstruction code format consists of how many bits?
(a) 5
(b) 4
(c) 7
(d) 2

Answer: Option (d)

—--

L2 Cache is a secondary cache in a computer system, which is larger but slower compared to L1 Cache.

L3 Cache is a tertiary cache in some systems, which is larger but slower compared to both L1 and L2 Caches.

This option is correct. L1 Cache, or Level 1 Cache, is the smallest and fastest cache in a computer system. It is located closest to the CPU and provides the fastest access to frequently used instructions and data.

—

RAM (Random Access Memory) is volatile memory used for temporary storage of data and instructions that the CPU needs to access quickly.

This option is correct. ROM (Read-Only Memory) is non-volatile memory used for long-term storage of data and instructions that are permanently stored and cannot be easily modified. It typically holds the firmware of devices and systems.

Cache Memory is volatile memory that acts as a buffer between the CPU and main memory (RAM), used to store frequently accessed data for faster retrieval by the CPU.

Hard Disk is a type of non-volatile secondary storage device used for long-term storage of data on a computer system, but it is not directly considered a type of memory.

—

In computer architecture, a pipeline refers to a technique where multiple stages of an instruction execution process are overlapped, allowing multiple instructions to be processed concurrently. This improves the throughput of instructions.

—

The system bus is responsible for connecting the CPU to external devices such as RAM and peripherals. It facilitates the transfer of data between these components, including addresses and control signals.

The control bus carries control signals that direct and coordinate activities within the computer's internal operations, such as memory access and I/O operations.

The address bus is used by the CPU to specify the address of a memory location or an I/O port. It is used for directing where data should be read from or written to.

The data bus is responsible for carrying data between the CPU, memory, and peripherals. It transfers actual data that needs to be processed or stored.

—-

In computer architecture, the term "word size" refers to the number of bits that the CPU processes in a single operation or the width of its internal registers. This size determines the amount of data that can be transferred internally between the CPU and RAM, and the size of instructions that the CPU can execute.

—

The Memory Management Unit (MMU) in a computer system is responsible for translating or mapping logical addresses generated by the CPU into physical addresses in RAM (Random Access Memory). This process allows programs to effectively access and utilize memory resources.

—

Bit Width: **Number of bits processed at once by the CPU**

—

Pipeline hazard: **Situations where instructions cannot execute in the pipeline due to conflicts**
—-

Bus width: Number of bits that can be transferred in a single bus cycle
—-

A superscalar processor is a type of CPU that executes multiple instructions simultaneously within a single clock cycle by exploiting instruction-level parallelism (ILP)
—

Ensuring consistency of data across multiple caches: cache coherence
–

Data Path: managing the data flow within the CPU
—

Immediate Addressing:
The operand itself is part of the instruction.

- **Example: `LOAD 5`, where 5 is the immediate operand.**

Direct Addressing:
The instruction contains the memory address where the operand is stored.

- **Example: `LOAD @100`, where 100 is the memory address.**

Indirect Addressing:
The instruction contains the address of a memory location that holds the address of the operand.

- **Example: `LOAD @(@200)`, where 200 is the address of a pointer that holds the address of the operand.**

Register Addressing:
The operand is located in a CPU register.

- **Example: `LOAD R1`, where R1 is a register.**

Indexed Addressing:
The effective address of the operand is calculated by adding a base address and an index.

- **Example: `LOAD ARRAY(R2)`, where R2 is an index and ARRAY is the base address.**

—-

1. Direct Mapping: Each main memory block is mapped to a specific cache line. This is the simplest but potentially least efficient method, as multiple memory blocks can map to the same cache line, leading to "thrashing".

2. Associative Mapping: Any main memory block can be stored in any cache line. This offers flexibility but requires more complex hardware to search the entire cache for a match.

3. Set-Associative Mapping: A compromise between direct and associative mapping, it divides the cache into sets, and each main memory block can be mapped to any line within its corresponding set. This improves performance over direct mapping by reducing thrashing while maintaining hardware efficiency compared to fully associative mapping.
—-

Operating System

1. What is an operating system?
a) interface between the hardware and application programs
b) collection of programs that manages hardware resources
c) system service provider to the application programs
d) all of the mentioned

Answer: d
Explanation: An Operating System acts as an intermediary between user/user applications/application programs and hardware. It is a program that manages hardware resources. It provides services to application programs.

2. What is the main function of the command interpreter?
a) to provide the interface between the API and application program
b) to handle the files in the operating system
c) to get and execute the next user-specified command
d) none of the mentioned

Answer: c
Explanation: The main function of a command interpreter is to get and execute the next user-specified command. Command Interpreter checks for valid command and then runs that command else it will throw an error.

3. In Operating Systems, which of the following is/are CPU scheduling algorithms?
a) Priority
b) Round Robin
c) Shortest Job First
d) All of the mentioned

Answer: d
Explanation: In Operating Systems, CPU scheduling algorithms are:

i) First Come First Served scheduling
ii) Shortest Job First scheduling
iii) Priority scheduling
iv) Round Robin scheduling
v) Multilevel Queue scheduling
vi) Multilevel Feedback Queue scheduling
All of these scheduling algorithms have their own advantages and disadvantages.

4. To access the services of the operating system, the interface is provided by the _____
a) Library
b) System calls
c) Assembly instructions
d) API

Answer: b
Explanation: To access services of the Operating System an interface is provided by the System Calls. Generally, these are functions written in C and C++. Open, Close, Read, Write are some of most prominently used system calls.

5. CPU scheduling is the basis of _____
a) multiprogramming operating systems
b) larger memory sized systems
c) multiprocessor systems
d) none of the mentioned

Answer: a
Explanation: None.

6. Which one of the following is not true?
a) kernel remains in the memory during the entire computer session
b) kernel is made of various modules which can not be loaded in running operating system
c) kernel is the first part of the operating system to load into memory during booting
d) kernel is the program that constitutes the central core of the operating system

Answer: b
Explanation: Kernel is the first program that is loaded in memory when OS is loading as well as it remains in memory till OS is running. Kernel is the core part of the OS which is responsible for managing resources, allowing multiple processes to use the resources and provide services to various processes. Kernel modules can be loaded and unloaded in run-time i.e. in running OS.

7. Which one of the following errors will be handle by the operating system?
a) lack of paper in printer
b) connection failure in the network
c) power failure
d) all of the mentioned

Answer: d
Explanation: All the mentioned errors are handled by OS. The OS is continuously monitoring all of its resources. Also, the OS is constantly detecting and correcting errors.

8. Where is the operating system placed in the memory?
a) either low or high memory (depending on the location of interrupt vector)
b) in the low memory
c) in the high memory
d) none of the mentioned

Answer: a
Explanation: None.

9. If a process fails, most operating system write the error information to a _____
a) new file
b) another running process
c) log file
d) none of the mentioned

Answer: c
Explanation: If a process fails, most operating systems write the error information to a log file. Log file is examined by the debugger, to find out what is the actual cause of that particular problem. Log file is useful for system programmers for correcting errors.

10. Which one of the following is not a real time operating system?
a) RTLinux
b) Palm OS
c) QNX
d) VxWorks

Answer: b
Explanation: VxWorks, QNX & RTLinux are real-time operating systems. Palm OS is a mobile operating system. Palm OS is developed for Personal Digital Assistants (PDAs).

11. What does OS X has?
a) monolithic kernel with modules
b) microkernel
c) monolithic kernel
d) hybrid kernel

Answer: d
Explanation: OS X has a hybrid kernel. Hybrid kernel is a combination of two different kernels. OS X is developed by Apple and originally it is known as Mac OS X.

12. In operating system, each process has its own _____
a) open files
b) pending alarms, signals, and signal handlers
c) address space and global variables
d) all of the mentioned

Answer: d
Explanation: In Operating Systems, each process has its own address space which contains code,

data, stack, and heap segments or sections. Each process also has a list of files that is opened by the process as well as all pending alarms, signals, and various signal handlers.

13. In a timeshare operating system, when the time slot assigned to a process is completed, the process switches from the current state to?
a) Suspended state
b) Terminated state
c) Ready state
d) Blocked state

Answer: c
Explanation: In a time-sharing operating system, when the time slot given to a process is completed, the process goes from the running state to the Ready State. In a time-sharing operating system, unit time is defined for sharing CPU, it is called a time quantum or time slice. If a process takes less than 1 time quantum, then the process itself releases the CPU.

14. Cascading termination refers to the termination of all child processes if the parent process terminates _____
a) Normally or abnormally
b) Abnormally
c) Normally
d) None of the mentioned

Answer: a
Explanation: Cascading termination refers to the termination of all child processes if the parent process terminates Normally or Abnormally. Some systems don't allow child processes to exist if the parent process has terminated. Cascading termination is normally initiated by the operating system.

15. When a process is in a "Blocked" state waiting for some I/O service. When the service is completed, it goes to the _____
a) Terminated state
b) Suspended state
c) Running state
d) Ready state

Answer: d
Explanation: Suppose that a process is in "Blocked" state waiting for some I/O service. When the service is completed, it goes to the ready state. Process never goes directly to the running state from the waiting state. Only processes which are in ready state go to the running state whenever CPU allocated by operating system.

16. Transient operating system code is a code that _____
a) stays in the memory always

b) never enters the memory space
c) comes and goes as needed
d) is not easily accessible

Answer: c
Explanation: None.

17. The portion of the process scheduler in an operating system that dispatches processes is concerned with _____
a) assigning ready processes to waiting queue
b) assigning running processes to blocked queue
c) assigning ready processes to CPU
d) all of the mentioned

Answer: c
Explanation: None.

18. The FCFS algorithm is particularly troublesome for _____
a) operating systems
b) multiprocessor systems
c) time sharing systems
d) multiprogramming systems

Answer: c
Explanation: In a time sharing system, each user needs to get a share of the CPU at regular intervals.

19. For an effective operating system, when to check for deadlock?
a) every time a resource request is made at fixed time intervals
b) at fixed time intervals
c) every time a resource request is made
d) none of the mentioned

Answer: a
Explanation: In an effective operating system, we must verify the deadlock each time a request for resources is made at fixed time intervals.

20. A deadlock avoidance algorithm dynamically examines the _____ to ensure that a circular wait condition can never exist.
a) operating system
b) resources
c) system storage state
d) resource allocation state

Answer: d
Explanation: Resource allocation states are used to maintain the availability of the already and current available resources.

21. Swapping _____ be done when a process has pending I/O, or has to execute I/O operations only into operating system buffers.
a) must never
b) maybe
c) can
d) must

Answer: a
Explanation: None.

22. The main memory accommodates _____
a) cpu
b) user processes
c) operating system
d) all of the mentioned

Answer: c
Explanation: None.

23. The operating system is responsible for?
a) bad-block recovery
b) booting from disk
c) disk initialization
d) all of the mentioned

Answer: d
Explanation: None.

24. The operating system and the other processes are protected from being modified by an already running process because _____
a) every address generated by the CPU is being checked against the relocation and limit registers
b) they have a protection algorithm
c) they are in different memory spaces
d) they are in different logical addresses

Answer: a
Explanation: None.

25. Using transient code, _____ the size of the operating system during program execution.
a) maintains
b) changes
c) increases
d) decreases

Answer: b
Explanation: None.

26. The operating system maintains a _____ table that keeps track of how many frames have been allocated, how many are there, and how many are available.
a) memory
b) mapping
c) page
d) frame

Answer: d
Explanation: None.

27. To obtain better memory utilization, dynamic loading is used. With dynamic loading, a routine is not loaded until it is called. For implementing dynamic loading _____
a) special support from operating system is essential
b) special support from hardware is required
c) user programs can implement dynamic loading without any special support from hardware or operating system
d) special support from both hardware and operating system is essential

Answer: c
Explanation: None.

28. The _____ presents a uniform device-access interface to the I/O subsystem, much as system calls provide a standard interface between the application and the operating system.
a) Device drivers
b) I/O systems
c) Devices
d) Buses

Answer: a
Explanation: None.

29. In real time operating system _____
a) process scheduling can be done only once
b) all processes have the same priority

c) kernel is not required
d) a task must be serviced by its deadline period

Answer: d
Explanation: None.

30. Hard real time operating system has _____ jitter than a soft real time operating system.
a) equal
b) more
c) less
d) none of the mentioned

Answer: c
Explanation: Jitter is the undesired deviation from the true periodicity.

31. For real time operating systems, interrupt latency should be _____
a) zero
b) minimal
c) maximum
d) dependent on the scheduling

Answer: b
Explanation: Interrupt latency is the time duration between the generation of interrupt and execution of its service.

32. Which one of the following is a real time operating system?
a) Windows CE
b) RTLinux
c) VxWorks
d) All of the mentioned

Answer: d
Explanation: None.

33. The priority of a process will _____ if the scheduler assigns it a static priority.
a) depends on the operating system
b) change
c) remain unchanged
d) none of the mentioned

Answer: c
Explanation: None.

34. What are the characteristics of Host based IDS?
a) Logs are analysed to detect tails of intrusion
b) The host operating system logs in the audit information
c) Logs includes logins, file opens, and program executions
d) All of the mentioned

Answer: d
Explanation: None.

35. What are the characteristics of stack based IDS?
a) It is programmed to interpret a certain series of packets
b) It models the normal usage of the network as a noise characterization
c) They are integrated closely with the TCP/IP stack and watch packets
d) The host operating system logs in the audit information

Answer: c
Explanation: None.

36. If the sum of the working – set sizes increases, exceeding the total number of available frames _____
a) the operating system selects a process to suspend
b) the system crashes
c) then the process crashes
d) the memory overflows

Answer: a
Explanation: None.

37. The information about all files is kept in _____
a) operating system
b) separate directory structure
c) swap space
d) none of the mentioned

Answer: b
Explanation: None.

38. The operating system keeps a small table containing information about all open files called _____
a) file table
b) directory table
c) open-file table
d) system table

Answer: c
Explanation: None.

39. What will happen in the single level directory?
a) All files are contained in the same directory
b) All files are contained in different directories all at the same level
c) Depends on the operating system
d) None of the mentioned

Answer: a
Explanation: None.

40. The operating system _____ the links when traversing directory trees, to preserve the acyclic structure of the system.
a) deletes
b) considers
c) ignores
d) none of the mentioned

Answer: c
Explanation: None.

41. To recover from failures in the network operations _____ information may be maintained.
a) operating system
b) ip address
c) stateless
d) state

Answer: d
Explanation: None.

42. On systems where there are multiple operating system, the decision to load a particular one is done by _____
a) process control block
b) file control block
c) boot loader
d) bootstrap

Answer: c
Explanation: None.

43. Whenever a process needs I/O to or from a disk it issues a _____
a) system call to the operating system
b) a special procedure
c) system call to the CPU
d) all of the mentioned

Answer: a
Explanation: None.

44. The two steps the operating system takes to use a disk to hold its files are _____ and _____
a) caching & logical formatting
b) logical formatting & swap space creation
c) swap space creation & caching
d) partitioning & logical formatting

Answer: d
Explanation: None.

45. The _____ program initializes all aspects of the system, from CPU registers to device controllers and the contents of main memory, and then starts the operating system.
a) bootstrap
b) main
c) bootloader
d) rom

Answer: a
Explanation: None.

46. In SCSI disks used in high end PCs, the controller maintains a list of _____ on the disk. The disk is initialized during _____ formatting which sets aside spare sectors not visible to the operating system.
a) destroyed blocks, partitioning
b) bad blocks, low level formatting
c) destroyed blocks, high level formatting
d) bad blocks, partitioning

Answer: b
Explanation: None.

47. Which principle states that programs, users, and even the systems be given just enough privileges to perform their task?
a) principle of least privilege

b) principle of process scheduling
c) principle of operating system
d) none of the mentioned

Answer: a
Explanation: None.

48. Network operating system runs on _____
a) every system in the network
b) server
c) both server and every system in the network
d) none of the mentioned

Answer: b
Explanation: None.

49. What are the types of distributed operating systems?
a) Zone based Operating system
b) Level based Operating system
c) Network Operating system
d) All of the mentioned

Answer: c
Explanation: None.

50. In Unix, which system call creates the new process?
a) create
b) fork
c) new
d) none of the mentioned

Answer: b
Explanation: In UNIX, a new process is created by fork() system call. fork() system call returns a process ID which is generally the process id of the child process created.

Process

1. The systems which allow only one process execution at a time, are called _____
a) uniprogramming systems
b) uniprocessing systems
c) unitasking systems
d) none of the mentioned

Answer: b
Explanation: Those systems which allow more than one process execution at a time, are called multiprocessing systems. Uniprocessing means only one processor.

2. In operating system, each process has its own _____
a) address space and global variables
b) open files
c) pending alarms, signals and signal handlers
d) all of the mentioned

Answer: d
Explanation: In Operating Systems, each process has its own address space which contains code, data, stack and heap segments or sections. Each process also has a list of files which is opened by the process as well as all pending alarms, signals and various signal handlers.

3. In Unix, Which system call creates the new process?
a) fork
b) create
c) new
d) none of the mentioned

Answer: a
Explanation: In UNIX, a new process is created by fork() system call. fork() system call returns a process ID which is generally the process id of the child process created.

4. A process can be terminated due to _____
a) normal exit
b) fatal error
c) killed by another process
d) all of the mentioned

Answer: d
Explanation: A process can be terminated normally by completing its task or because of fatal error or killed by another process or forcefully killed by a user. When the process completes its task without any error then it exits normally. The process may exit abnormally because of the occurrence of fatal error while it is running. The process can be killed or terminated forcefully by another process.

5. What is the ready state of a process?
a) when process is scheduled to run after some execution
b) when process is unable to run until some task has been completed
c) when process is using the CPU
d) none of the mentioned

Answer: a
Explanation: Ready state of the process means process has all necessary resources which are required for execution of that process when CPU is allocated. Process is ready for execution but waiting for the CPU to be allocated.

6. What is interprocess communication?
a) communication within the process
b) communication between two process
c) communication between two threads of same process
d) none of the mentioned

Answer: b
Explanation: Interprocess Communication (IPC) is a communication mechanism that allows processes to communicate with each other and synchronise their actions without using the same address space. IPC can be achieved using shared memory and message passing.

7. A set of processes is deadlock if _____
a) each process is blocked and will remain so forever
b) each process is terminated
c) all processes are trying to kill each other
d) none of the mentioned

Answer: a
Explanation: Deadlock is a situation which occurs because process A is waiting for one resource and holds another resource (blocking resource). At the same time another process B demands blocking a resource as it is already held by a process A, process B is waiting state unless and until process A releases occupied resource.

8. A process stack does not contain _____
a) Function parameters
b) Local variables
c) Return addresses
d) PID of child process

Answer: d
Explanation: Process stack contains Function parameters, Local variables and Return address. It does not contain the PID of child process.

9. Which system call can be used by a parent process to determine the termination of child process?
a) wait
b) exit
c) fork
d) get

Answer: a
Explanation: wait() system call is used by the parent process to determine termination of child process. The parent process uses wait() system call and gets the exit status of the child process as well as the pid of the child process which is terminated.

10. The address of the next instruction to be executed by the current process is provided by the _____
a) CPU registers
b) Program counter
c) Process stack
d) Pipe

Answer: b
Explanation: The address of the next instruction to be executed by the current process is provided by the Program Counter. After every instruction is executed, the Program Counter is incremented by 1 i.e. address of the next instruction to be executed. CPU fetches instruction from the address denoted by Program Counter and execute it.

1. A Process Control Block(PCB) does not contain which of the following?
a) Code
b) Stack
c) Bootstrap program
d) Data

Answer: c
Explanation: Process Control Block (PCB) contains information related to a process such as Process State, Program Counter, CPU Register, etc. Process Control Block is also known as Task Control Block. Bootstrap program is a program which runs initially when the system or computer is booted or rebooted.

2. The number of processes completed per unit time is known as _____
a) Output
b) Throughput
c) Efficiency
d) Capacity

Answer: b
Explanation: The number of processes completed per unit time is known as Throughput. Suppose there are 4 processes A, B, C & D they are taking 1, 3, 4 & 7 units of time respectively for their executions. For 10 units of time, throughput is high if process A, B & C are running first as 3 processes can execute. If process C runs first then throughput is low as maximum only 2 processes can execute. Throughput is low for processes which take a long time for execution. Throughput is high for processes which take a short time for execution.

3. The state of a process is defined by _____
a) the final activity of the process
b) the activity just executed by the process
c) the activity to next be executed by the process
d) the current activity of the process

Answer: d
Explanation: The state of a process is defined by the current activity of the process. A process state changes when the process executes. The process states are as New, Ready, Running, Wait, Terminated.

4. Which of the following is not the state of a process?
a) New
b) Old
c) Waiting
d) Running

Answer: b
Explanation: There is no process state such as old. When a process is created then the process is in New state. When the process gets the CPU for its execution then the process is in Running state. When the process is waiting for an external event then the process is in a Waiting state.

5. What is a Process Control Block?
a) Process type variable
b) Data Structure
c) A secondary storage section
d) A Block in memory

Answer: b
Explanation: A Process Control Block (PCB) is a data structure. It contains information related to a process such as Process State, Program Counter, CPU Register, etc. Process Control Block is also known as Task Control Block.

6. The entry of all the PCBs of the current processes is in _____
a) Process Register
b) Program Counter
c) Process Table
d) Process Unit

Answer: c
Explanation: The entry of all the PCBs of the current processes is in Process Table. The Process Table has the status of each and every process that is created in OS along with their PIDs.

7. What is the degree of multiprogramming?
a) the number of processes executed per unit time
b) the number of processes in the ready queue
c) the number of processes in the I/O queue
d) the number of processes in memory

Answer: d
Explanation: Multiprogramming means the number of processes are in the ready states. To increase utilization of CPU, Multiprogramming is one of the most important abilities of OS. Generally, a single process cannot use CPU or I/O at all time, whenever CPU or I/O is available another process can use it. By doing this CPU utilization is increased.

8. A single thread of control allows the process to perform _____
a) only one task at a time
b) multiple tasks at a time
c) only two tasks at a time
d) all of the mentioned

Answer: a
Explanation: A single thread of control allows the process to perform only one task at a time. In the case of multi-core, multiple threads can be run simultaneously and can perform multiple tasks at a time.

9. What is the objective of multiprogramming?
a) Have a process running at all time
b) Have multiple programs waiting in a queue ready to run
c) To increase CPU utilization
d) None of the mentioned

Answer: c
Explanation: The objective of multiprogramming is to increase CPU utilization. Generally, a single process cannot use CPU or I/O at all time, whenever CPU or I/O is available another process can use it. Multiprogramming offers this ability to OS by keeping multiple programs in a ready queue.

Synchonization

1. Which process can be affected by other processes executing in the system?
a) cooperating process
b) child process
c) parent process
d) init process

Answer: a
Explanation: A cooperating process can be affected by other processes executing in the system. Also it can affect other processes executing in the system. A process shares data with other processes, such a process is known as a cooperating process.

2. When several processes access the same data concurrently and the outcome of the execution depends on the particular order in which the access takes place is called _____
a) dynamic condition
b) race condition
c) essential condition
d) critical condition

Answer: b
Explanation: When several processes access the same data concurrently and the outcome of the execution depends on the particular order in which access takes place is called race condition.

3. If a process is executing in its critical section, then no other processes can be executing in their critical section. What is this condition called?
a) mutual exclusion
b) critical exclusion
c) synchronous exclusion
d) asynchronous exclusion

Answer: a
Explanation: If a process is executing in its critical section, then no other processes can be executed in their critical section. This condition is called Mutual Exclusion. Critical section of the process is shared between multiple processes. If this section is executed by more than one or all of them concurrently then the outcome of this is not as per desired outcome. For this reason the critical section of the process should not be executed concurrently.

4. Which one of the following is a synchronization tool?
a) thread
b) pipe
c) semaphore
d) socket

Answer: c
Explanation: Semaphore is a synchronization tool. Semaphore is a mechanism which synchronizes or controls access of threads on critical resources. There are two types of semaphores i) Binary Semaphore ii) Counting Semaphore.

5. A semaphore is a shared integer variable _____
a) that can not drop below zero

b) that can not be more than zero
c) that can not drop below one
d) that can not be more than one

Answer: a
Explanation: A semaphore is a shared integer variable that can not drop below zero. In binary semaphore, if the value of the semaphore variable is zero that means there is a process that uses a critical resource and no other process can access the same critical resource until it is released. In Counting semaphore, if the value of the semaphore variable is zero that means there is no resource available.

6. Mutual exclusion can be provided by the _____
a) mutex locks
b) binary semaphores
c) both mutex locks and binary semaphores
d) none of the mentioned

Answer: c
Explanation: Mutual exclusion can be provided by both mutex locks and binary semaphore. Mutex is a short form of **Mut**ual **Ex**clusion. Binary semaphore also provides a mechanism for mutual exclusion. Binary semaphore behaves similar to mutex locks.

7. When high priority task is indirectly preempted by medium priority task effectively inverting the relative priority of the two tasks, the scenario is called _____
a) priority inversion
b) priority removal
c) priority exchange
d) priority modification

Answer: a
Explanation: When a high priority task is indirectly preempted by a medium priority task effectively inverting the relative priority of the two tasks, the scenario is called priority inversion.

8. Process synchronization can be done on _____
a) hardware level
b) software level
c) both hardware and software level
d) none of the mentioned

Answer: c
Explanation: Process synchronization can be done on both hardware and software level. Critical section problems can be resolved using hardware synchronisation. But this method is not simple for implementation so software synchronization is mostly used.

9. A monitor is a module that encapsulates _____
a) shared data structures
b) procedures that operate on shared data structure
c) synchronization between concurrent procedure invocation
d) all of the mentioned

Answer: d
Explanation: A monitor is a module that encapsulates shared data structures, procedures that operate on shared data structure, synchronization between concurrent procedure invocation.

10. To enable a process to wait within the monitor _____
a) a condition variable must be declared as condition
b) condition variables must be used as boolean objects
c) semaphore must be used
d) all of the mentioned

Answer: a
Explanation: To enable a process to wait within the monitor a condition variable must be declared as condition.

1. The bounded buffer problem is also known as _____
a) Readers – Writers problem
b) Dining – Philosophers problem
c) Producer – Consumer problem
d) None of the mentioned

Answer: c
Explanation: None.

2. In the bounded buffer problem, there are the empty and full semaphores that
a) count the number of empty and full buffers
b) count the number of empty and full memory spaces
c) count the number of empty and full queues
d) none of the mentioned

Answer: a
Explanation: None.

3. In the bounded buffer problem _____
a) there is only one buffer
b) there are n buffers (n being greater than one but finite)
c) there are infinite buffers
d) the buffer size is bounded

Answer: b
Explanation: None.

4. To ensure difficulties do not arise in the readers – writers problem _____ are given exclusive access to the shared object.
a) readers
b) writers
c) readers and writers
d) none of the mentioned

Answer: b
Explanation: None.

5. The dining – philosophers problem will occur in case of _____
a) 5 philosophers and 5 chopsticks
b) 4 philosophers and 5 chopsticks
c) 3 philosophers and 5 chopsticks
d) 6 philosophers and 5 chopsticks

Answer: a
Explanation: None.

6. A deadlock free solution to the dining philosophers problem _____
a) necessarily eliminates the possibility of starvation
b) does not necessarily eliminate the possibility of starvation
c) eliminates any possibility of any kind of problem further
d) none of the mentioned

Answer: b
Explanation: None.

3. Semaphore is a/an _____ to solve the critical section problem.
a) hardware for a system
b) special program for a system
c) integer variable
d) none of the mentioned

Answer: c

1. An un-interruptible unit is known as _____
a) single
b) atomic

c) static
d) none of the mentioned

Answer: b

2. TestAndSet instruction is executed _____
a) after a particular process
b) periodically
c) atomically
d) none of the mentioned

Answer: c

3. Semaphore is a/an _____ to solve the critical section problem.
a) hardware for a system
b) special program for a system
c) integer variable
d) none of the mentioned

Answer: c

4. What are the two atomic operations permissible on semaphores?
a) wait and signal
b) stop and wait
c) hold and signal
d) none of the mentioned

Answer: a

5. What are Spinlocks?
a) CPU cycles wasting locks over critical sections of programs
b) Locks that avoid time wastage in context switches
c) Locks that work better on multiprocessor systems
d) All of the mentioned

Answer: d

6. What is the main disadvantage of spinlocks?
a) they are not sufficient for many process
b) they require busy waiting
c) they are unreliable sometimes
d) they are too complex for programmers

Answer: b

7. The wait operation of the semaphore basically works on the basic _____ system call.
a) stop()
b) block()
c) hold()
d) wait()

Answer: b

8. The signal operation of the semaphore basically works on the basic _____ system call.
a) continue()
b) wakeup()
c) getup()
d) start()

Answer: b

9. If the semaphore value is negative _____
a) its magnitude is the number of processes waiting on that semaphore
b) it is invalid
c) no operation can be further performed on it until the signal operation is performed on it
d) none of the mentioned

Answer: a

10. The code that changes the value of the semaphore is _____
a) remainder section code
b) non – critical section code
c) critical section code
d) none of the mentioned

Answer: c

.1. A collection of instructions that performs a single logical function is called _____
a) transaction
b) operation
c) function
d) all of the mentioned

Answer: a

2. A terminated transaction that has completed its execution successfully is _____ otherwise it is _____
a) committed, destroyed
b) aborted, destroyed
c) committed, aborted
d) none of the mentioned

Answer: c

3. The state of the data accessed by an aborted transaction must be restored to what it was just before the transaction started executing. This restoration is known as _____ of transaction.
a) safety
b) protection
c) roll – back
d) revert – back

Answer: c

4. Write ahead logging is a way _____
a) to ensure atomicity
b) to keep data consistent
c) that records data on stable storage
d) all of the mentioned

Answer: d

5. In the write ahead logging a _____ is maintained.
a) a memory
b) a system
c) a disk
d) a log record

Answer: d

6. An actual update is not allowed to a data item _____
a) before the corresponding log record is written out to stable storage
b) after the corresponding log record is written out to stable storage
c) until the whole log record has been checked for inconsistencies
d) all of the mentioned

Answer: a

7. The undo and redo operations must be _____ to guarantee correct behaviour, even if a failure occurs during recovery process.
a) idempotent
b) easy
c) protected
d) all of the mentioned

Answer: a
Explanation: Idempotent – Multiple executions of an operation have the same result as does one execution.

8. The system periodically performs checkpoints that consists of the following operation(s)
a) Putting all the log records currently in main memory onto stable storage
b) putting all modified data residing in main memory onto stable storage
c) putting a log record onto stable storage
d) all of the mentioned

Answer: d

9. Consider a transaction T1 that committed prior to checkpoint. The <T1 commits> record appears in the log before the <checkpoint> record. Any modifications made by T1 must have been written to the stable storage either with the checkpoint or prior to it. Thus at recovery time _____
a) There is a need to perform an undo operation on T1
b) There is a need to perform a redo operation on T1
c) There is no need to perform an undo and redo operation on T1
d) All of the mentioned

Answer: c

10. Serializable schedules are ones where _____
a) concurrent execution of transactions is equivalent to the transactions executed serially
b) the transactions can be carried out one after the other
c) a valid result occurs after execution transactions
d) none of the mentioned

Answer: a

11. A locking protocol is one that _____
a) governs how locks are acquired
b) governs how locks are released
c) governs how locks are acquired and released
d) none of the mentioned

Answer: c

12. The two phase locking protocol consists of _____
a) growing & shrinking phase
b) shrinking & creation phase
c) creation & growing phase
d) destruction & creation phase

Answer: a

13. The growing phase is a phase in which?
a) A transaction may obtain locks, but does not release any
b) A transaction may obtain locks, and releases a few or all of them
c) A transaction may release locks, but does not obtain any new locks
d) A transaction may release locks, and does obtain new locks

Answer: a

14. The shrinking phase is a phase in which?
a) A transaction may obtain locks, but does not release any
b) A transaction may obtain locks, and releases a few or all of them
c) A transaction may release locks, but does not obtain any new locks
d) A transaction may release locks, and does obtain new locks

Answer: c

15. Which of the following concurrency control protocols ensure both conflict serializability and freedom from deadlock?
I) 2-phase locking
II) Timestamp ordering
a) I only
b) II only
c) Both I and II
d) Neither I nor II

Answer: b

Scheduling

1. Which module gives control of the CPU to the process selected by the short-term scheduler?
a) dispatcher

b) interrupt
c) scheduler
d) none of the mentioned

Answer: a

2. The processes that are residing in main memory and are ready and waiting to execute are kept on a list called _____
a) job queue
b) ready queue
c) execution queue
d) process queue

Answer: b

3. The interval from the time of submission of a process to the time of completion is termed as _____
a) waiting time
b) turnaround time
c) response time
d) throughput

Answer: b

4. Which scheduling algorithm allocates the CPU first to the process that requests the CPU first?
a) first-come, first-served scheduling
b) shortest job scheduling
c) priority scheduling
d) none of the mentioned

Answer: a

5. In priority scheduling algorithm _____
a) CPU is allocated to the process with highest priority
b) CPU is allocated to the process with lowest priority
c) Equal priority processes can not be scheduled
d) None of the mentioned

Answer: a

6. In priority scheduling algorithm, when a process arrives at the ready queue, its priority is compared with the priority of _____

a) all process
b) currently running process
c) parent process
d) init process

Answer: b

7. Which algorithm is defined in Time quantum?
a) shortest job scheduling algorithm
b) round robin scheduling algorithm
c) priority scheduling algorithm
d) multilevel queue scheduling algorithm

Answer: b

8. Process are classified into different groups in _____
a) shortest job scheduling algorithm
b) round robin scheduling algorithm
c) priority scheduling algorithm
d) multilevel queue scheduling algorithm

Answer: d

9. In multilevel feedback scheduling algorithm _____
a) a process can move to a different classified ready queue
b) classification of ready queue is permanent
c) processes are not classified into groups
d) none of the mentioned

Answer: a

10. Which one of the following can not be scheduled by the kernel?
a) kernel level thread
b) user level thread
c) process
d) none of the mentioned

Answer: b
Explanation: User level threads are managed by thread library and the kernel is unaware of them.

1. CPU scheduling is the basis of _____
a) multiprocessor systems

b) multiprogramming operating systems
c) larger memory sized systems
d) none of the mentioned

Answer: b

2. With multiprogramming _____ is used productively.
a) time
b) space
c) money
d) all of the mentioned

Answer: a

3. What are the two steps of a process execution?
a) I/O & OS Burst
b) CPU & I/O Burst
c) Memory & I/O Burst
d) OS & Memory Burst

Answer: b

4. An I/O bound program will typically have _____
a) a few very short CPU bursts
b) many very short I/O bursts
c) many very short CPU bursts
d) a few very short I/O bursts

Answer: c
Explanation: An I/O bound program frequently performs short computations (short CPU bursts) followed by waiting for I/O operations to complete.

5. A process is selected from the _____ queue by the _____ scheduler, to be executed.
a) blocked, short term
b) wait, long term
c) ready, short term
d) ready, long term

Answer: c

6. In the following cases non – preemptive scheduling occurs?
a) When a process switches from the running state to the ready state

b) When a process goes from the running state to the waiting state
c) When a process switches from the waiting state to the ready state
d) All of the mentioned

Answer: b
Explanation: There is no other choice.

7. The switching of the CPU from one process or thread to another is called _____
a) process switch
b) task switch
c) context switch
d) all of the mentioned

Answer: c

8. What is Dispatch latency?
a) the speed of dispatching a process from running to the ready state
b) the time of dispatching a process from running to ready state and keeping the CPU idle
c) the time to stop one process and start running another one
d) none of the mentioned

Answer: c

9. Scheduling is done so as to _____
a) increase CPU utilization
b) decrease CPU utilization
c) keep the CPU more idle
d) none of the mentioned

Answer: a

10. Scheduling is done so as to _____
a) increase the throughput
b) decrease the throughput
c) increase the duration of a specific amount of work
d) none of the mentioned

Answer: a

11. What is Turnaround time?
a) the total waiting time for a process to finish execution
b) the total time spent in the ready queue

c) the total time spent in the running queue
d) the total time from the completion till the submission of a process

Answer: d

12. Scheduling is done so as to _____
a) increase the turnaround time
b) decrease the turnaround time
c) keep the turnaround time same
d) there is no relation between scheduling and turnaround time

Answer: b

13. What is Waiting time?
a) the total time in the blocked and waiting queues
b) the total time spent in the ready queue
c) the total time spent in the running queue
d) the total time from the completion till the submission of a process

Answer: b

14. Scheduling is done so as to _____
a) increase the waiting time
b) keep the waiting time the same
c) decrease the waiting time
d) none of the mentioned

Answer: c

15. What is Response time?
a) the total time taken from the submission time till the completion time
b) the total time taken from the submission time till the first response is produced
c) the total time taken from submission time till the response is output
d) none of the mentioned

Answer: b

1. Which is the most optimal scheduling algorithm?
a) FCFS – First come First served
b) SJF – Shortest Job First

c) RR – Round Robin
d) None of the mentioned

Answer: b

2. The real difficulty with SJF in short term scheduling is _____
a) it is too good an algorithm
b) knowing the length of the next CPU request
c) it is too complex to understand
d) none of the mentioned

Answer: b

3. The FCFS algorithm is particularly troublesome for _____
a) time sharing systems
b) multiprogramming systems
c) multiprocessor systems
d) operating systems

Answer: a
Explanation: In a time sharing system, each user needs to get a share of the CPU at regular intervals.

4. Consider the following set of processes, the length of the CPU burst time given in milliseconds.

Process	Burst time
P1	6
P2	8
P3	7
P4	3

Assuming the above process being scheduled with the SJF scheduling algorithm.
a) The waiting time for process P1 is 3ms
b) The waiting time for process P1 is 0ms
c) The waiting time for process P1 is 16ms
d) The waiting time for process P1 is 9ms

Answer: a

5. Preemptive Shortest Job First scheduling is sometimes called _____
a) Fast SJF scheduling
b) EDF scheduling – Earliest Deadline First
c) HRRN scheduling – Highest Response Ratio Next
d) SRTN scheduling – Shortest Remaining Time Next

Answer: d

6. An SJF algorithm is simply a priority algorithm where the priority is _____
a) the predicted next CPU burst
b) the inverse of the predicted next CPU burst
c) the current CPU burst
d) anything the user wants

Answer: a
Explanation: The larger the CPU burst, the lower the priority.

7. Choose one of the disadvantages of the priority scheduling algorithm?
a) it schedules in a very complex manner
b) its scheduling takes up a lot of time
c) it can lead to some low priority process waiting indefinitely for the CPU
d) none of the mentioned

Answer: c

8. What is ‘Aging’?
a) keeping track of cache contents
b) keeping track of what pages are currently residing in memory
c) keeping track of how many times a given page is referenced
d) increasing the priority of jobs to ensure termination in a finite time

Answer: d

9. A solution to the problem of indefinite blockage of low – priority processes is _____
a) Starvation
b) Wait queue
c) Ready queue
d) Aging

Answer: d

10. Which of the following statements are true? (GATE 2010)

i) Shortest remaining time first scheduling may cause starvation
ii) Preemptive scheduling may cause starvation
iii) Round robin is better than FCFS in terms of response time
a) i only
b) i and iii only
c) ii and iii only
d) i, ii and iii

Answer: d

11. Which of the following scheduling algorithms gives minimum average waiting time?
a) FCFS
b) SJF
c) Round – robin
d) Priority

Answer: b

1. Concurrent access to shared data may result in _____
a) data consistency
b) data insecurity
c) data inconsistency
d) none of the mentioned

Answer: c

2. A situation where several processes access and manipulate the same data concurrently and the outcome of the execution depends on the particular order in which access takes place is called _____
a) data consistency
b) race condition
c) aging
d) starvation

Answer: b

3. The segment of code in which the process may change common variables, update tables, write into files is known as _____
a) program
b) critical section

c) non – critical section
d) synchronizing

Answer: b

4. Which of the following conditions must be satisfied to solve the critical section problem?
a) Mutual Exclusion
b) Progress
c) Bounded Waiting
d) All of the mentioned

Answer: d

5. Mutual exclusion implies that _____
a) if a process is executing in its critical section, then no other process must be executing in their critical sections
b) if a process is executing in its critical section, then other processes must be executing in their critical sections
c) if a process is executing in its critical section, then all the resources of the system must be blocked until it finishes execution
d) none of the mentioned

Answer: a

6. Bounded waiting implies that there exists a bound on the number of times a process is allowed to enter its critical section _____
a) after a process has made a request to enter its critical section and before the request is granted
b) when another process is in its critical section
c) before a process has made a request to enter its critical section
d) none of the mentioned

Answer: a

7. A minimum of _____ variable(s) is/are required to be shared between processes to solve the critical section problem.
a) one
b) two
c) three
d) four

Answer: b

8. In the bakery algorithm to solve the critical section problem _____
a) each process is put into a queue and picked up in an ordered manner
b) each process receives a number (may or may not be unique) and the one with the lowest number is served next
c) each process gets a unique number and the one with the highest number is served next
d) each process gets a unique number and the one with the lowest number is served next

Answer: b

2.If the wait for graph contains a cycle _____
(a) then a deadlock does not exist
(b) then a deadlock exists
(c) then the system is in a safe state
(d) either deadlock exists or system is in a safe state

Answer: Option (b)

Deadlock prevention

1. The number of resources requested by a process _____
a) must always be less than the total number of resources available in the system
b) must always be equal to the total number of resources available in the system
c) must not exceed the total number of resources available in the system
d) must exceed the total number of resources available in the system

Answer: c

2. The request and release of resources are _____
a) command line statements
b) interrupts
c) system calls
d) special programs

Answer: c

3. What are Multithreaded programs?
a) lesser prone to deadlocks
b) more prone to deadlocks

c) not at all prone to deadlocks
d) none of the mentioned

Answer: b
Explanation: Multiple threads can compete for shared resources.

4. For a deadlock to arise, which of the following conditions must hold simultaneously?
a) Mutual exclusion
b) No preemption
c) Hold and wait
d) All of the mentioned

Answer: d

5. For Mutual exclusion to prevail in the system _____
a) at least one resource must be held in a non sharable mode
b) the processor must be a uniprocessor rather than a multiprocessor
c) there must be at least one resource in a sharable mode
d) all of the mentioned

Answer: a
Explanation: If another process requests that resource (non – shareable resource), the requesting process must be delayed until the resource has been released.

6. For a Hold and wait condition to prevail _____
a) A process must be not be holding a resource, but waiting for one to be freed, and then request to acquire it
b) A process must be holding at least one resource and waiting to acquire additional resources that are being held by other processes
c) A process must hold at least one resource and not be waiting to acquire additional resources
d) None of the mentioned

Answer: b

7. Deadlock prevention is a set of methods _____
a) to ensure that at least one of the necessary conditions cannot hold
b) to ensure that all of the necessary conditions do not hold
c) to decide if the requested resources for a process have to be given or not
d) to recover from a deadlock

Answer: a

8. For non sharable resources like a printer, mutual exclusion _____
a) must exist
b) must not exist
c) may exist
d) none of the mentioned

Answer: a
Explanation: A printer cannot be simultaneously shared by several processes.

9. For sharable resources, mutual exclusion _____
a) is required
b) is not required
c) may be or may not be required
d) none of the mentioned

Answer: b
Explanation: They do not require mutually exclusive access, and hence cannot be involved in a deadlock.

10. To ensure that the hold and wait condition never occurs in the system, it must be ensured that _____
a) whenever a resource is requested by a process, it is not holding any other resources
b) each process must request and be allocated all its resources before it begins its execution
c) a process can request resources only when it has none
d) all of the mentioned

Answer: d
Explanation: c – A process may request some resources and use them. Before it can can request any additional resources, however it must release all the resources that it is currently allocated.

11. The disadvantage of a process being allocated all its resources before beginning its execution is _____
a) Low CPU utilization
b) Low resource utilization
c) Very high resource utilization
d) None of the mentioned

Answer: b

12. To ensure no preemption, if a process is holding some resources and requests another resource that cannot be immediately allocated to it _____
a) then the process waits for the resources be allocated to it
b) the process keeps sending requests until the resource is allocated to it

c) the process resumes execution without the resource being allocated to it
d) then all resources currently being held are preempted

Answer: d

13. One way to ensure that the circular wait condition never holds is to _____
a) impose a total ordering of all resource types and to determine whether one precedes another in the ordering
b) to never let a process acquire resources that are held by other processes
c) to let a process wait for only one resource at a time
d) all of the mentioned

Answer: a

Deadlock Avoidance

1. Each request requires that the system consider the _____ to decide whether the current request can be satisfied or must wait to avoid a future possible deadlock.
a) resources currently available
b) processes that have previously been in the system
c) resources currently allocated to each process
d) future requests and releases of each process

Answer: a

2. Given a priori information about the _____ number of resources of each type that maybe requested for each process, it is possible to construct an algorithm that ensures that the system will never enter a deadlock state.
a) minimum
b) average
c) maximum
d) approximate

Answer: c

3. A deadlock avoidance algorithm dynamically examines the _____ to ensure that a circular wait condition can never exist.
a) resource allocation state
b) system storage state
c) operating system
d) resources

Answer: a
Explanation: Resource allocation states are used to maintain the availability of the already and current available resources.

4. A state is safe, if _____
a) the system does not crash due to deadlock occurrence
b) the system can allocate resources to each process in some order and still avoid a deadlock
c) the state keeps the system protected and safe
d) all of the mentioned

Answer: b

5. A system is in a safe state only if there exists a _____
a) safe allocation
b) safe resource
c) safe sequence
d) all of the mentioned

Answer: c

6. All unsafe states are _____
a) deadlocks
b) not deadlocks
c) fatal
d) none of the mentioned

Answer: b

7. A system has 12 magnetic tape drives and 3 processes : P0, P1, and P2. Process P0 requires 10 tape drives, P1 requires 4 and P2 requires 9 tape drives.

Process
P0
P1
P2

Maximum needs (process-wise: P0 through P2 top to bottom)
10
4
9

Currently allocated (process-wise)
5

2
2
Which of the following sequence is a safe sequence?
a) P0, P1, P2
b) P1, P2, P0
c) P2, P0, P1
d) P1, P0, P2

Answer: d

8. If no cycle exists in the resource allocation graph _____
a) then the system will not be in a safe state
b) then the system will be in a safe state
c) all of the mentioned
d) none of the mentioned

Answer: b

9. The resource allocation graph is not applicable to a resource allocation system _____
a) with multiple instances of each resource type
b) with a single instance of each resource type
c) single & multiple instances of each resource type
d) none of the mentioned

Answer: a

10. The Banker's algorithm is _____ than the resource allocation graph algorithm.
a) less efficient
b) more efficient
c) equal
d) none of the mentioned

Answer: a

11. The data structures available in the Banker's algorithm are _____
a) Available
b) Need
c) Allocation
d) All of the mentioned

Answer: d

12. The content of the matrix Need is _____
a) Allocation – Available
b) Max – Available
c) Max – Allocation
d) Allocation – Max

Answer: c

Deadlock Detection

1. The wait-for graph is a deadlock detection algorithm that is applicable when _____
a) all resources have a single instance
b) all resources have multiple instances
c) all resources have a single 7 multiple instances
d) all of the mentioned

Answer: a

2. An edge from process Pi to Pj in a wait for graph indicates that _____
a) Pi is waiting for Pj to release a resource that Pi needs
b) Pj is waiting for Pi to release a resource that Pj needs
c) Pi is waiting for Pj to leave the system
d) Pj is waiting for Pi to leave the system

Answer: a

3. If the wait for graph contains a cycle _____
a) then a deadlock does not exist
b) then a deadlock exists
c) then the system is in a safe state
d) either deadlock exists or system is in a safe state

Answer: b

4. If deadlocks occur frequently, the detection algorithm must be invoked _____
a) rarely
b) frequently
c) rarely & frequently
d) none of the mentioned

Answer: b

5. What is the disadvantage of invoking the detection algorithm for every request?
a) overhead of the detection algorithm due to consumption of memory
b) excessive time consumed in the request to be allocated memory
c) considerable overhead in computation time
d) all of the mentioned

Answer: C

6. A deadlock eventually cripples system throughput and will cause the CPU utilization to _____
a) increase
b) drop
c) stay still
d) none of the mentioned

Answer: b

7. Every time a request for allocation cannot be granted immediately, the detection algorithm is invoked. This will help identify _____
a) the set of processes that have been deadlocked
b) the set of processes in the deadlock queue
c) the specific process that caused the deadlock
d) all of the mentioned

Answer: a

8. A computer system has 6 tape drives, with ‘n’ processes competing for them. Each process may need 3 tape drives. The maximum value of ‘n’ for which the system is guaranteed to be deadlock free is?
a) 2
b) 3
c) 4
d) 1

Answer: a

9. A system has 3 processes sharing 4 resources. If each process needs a maximum of 2 units then, deadlock _____
a) can never occur
b) may occur
c) has to occur
d) none of the mentioned

Answer: a

10. ‘m’ processes share ‘n’ resources of the same type. The maximum need of each process doesn’t exceed ‘n’ and the sum of all their maximum needs is always less than m+n. In this setup, deadlock _____

a) can never occur
b) may occur
c) has to occur
d) none of the mentioned

Answer: a

Deadlock Recovery

1. A deadlock can be broken by _____
a) abort one or more processes to break the circular wait
b) abort all the process in the system
c) preempt all resources from all processes
d) none of the mentioned

Answer: a

2. The two ways of aborting processes and eliminating deadlocks are _____
a) Abort all deadlocked processes
b) Abort all processes
c) Abort one process at a time until the deadlock cycle is eliminated
d) All of the mentioned

Answer: c

3. Those processes should be aborted on occurrence of a deadlock, the termination of which?
a) is more time consuming
b) incurs minimum cost
c) safety is not hampered
d) all of the mentioned

Answer: b

4. The process to be aborted is chosen on the basis of the following factors?
a) priority of the process
b) process is interactive or batch
c) how long the process has computed
d) all of the mentioned

Answer: d

5. Cost factors for process termination include _____
a) Number of resources the deadlock process is not holding
b) CPU utilization at the time of deadlock
c) Amount of time a deadlocked process has thus far consumed during its execution
d) All of the mentioned

Answer: c

6. If we preempt a resource from a process, the process cannot continue with its normal execution and it must be _____
a) aborted
b) rolled back
c) terminated
d) queued

Answer: b

7. To _____ to a safe state, the system needs to keep more information about the states of processes.
a) abort the process
b) roll back the process
c) queue the process
d) none of the mentioned

Answer: b

8. If the resources are always preempted from the same process _____ can occur.
a) deadlock
b) system crash
c) aging
d) starvation

Answer: d

9. What is the solution to starvation?
a) the number of rollbacks must be included in the cost factor
b) the number of resources must be included in resource preemption
c) resource preemption be done instead
d) all of the mentioned

Answer: a

Database - Models

1. A relational database consists of a collection of
a) Tables
b) Fields
c) Records
d) Keys

Answer: a
Explanation: Fields are the column of the relation or tables. Records are each row in a relation. Keys are the constraints in a relation.

2. A _____ in a table represents a relationship among a set of values.
a) Column
b) Key
c) Row
d) Entry

Answer: c
Explanation: Column has only one set of values. Keys are constraints and row is one whole set of attributes. Entry is just a piece of data.

3. The term _____ is used to refer to a row.
a) Attribute
b) Tuple
c) Field
d) Instance

Answer: b
Explanation: Tuple is one entry of the relation with several attributes which are fields.

4. The term attribute refers to a _____ of a table.
a) Record
b) Column
c) Tuple
d) Key

Answer: b
Explanation: Attribute is a specific domain in the relation which has entries of all tuples.

5. For each attribute of a relation, there is a set of permitted values, called the _____ of that attribute.
a) Domain
b) Relation
c) Set
d) Schema

Answer: a
Explanation: The values of the attribute should be present in the domain. Domain is a set of values permitted.

6. Database _____ which is the logical design of the database, and the database _____ which is a snapshot of the data in the database at a given instant in time.
a) Instance, Schema
b) Relation, Schema
c) Relation, Domain
d) Schema, Instance

Answer: d
Explanation: Instance is an instance of time and schema is a representation.

7. Course(course_id,sec_id,semester)
Here the course_id,sec_id and semester are _____ and course is a _____
a) Relations, Attribute
b) Attributes, Relation
c) Tuple, Relation
d) Tuple, Attributes

Answer: b
Explanation: The relation course has a set of attributes course_id,sec_id,semester .

8. Department (dept name, building, budget) and Employee (employee_id, name, dept name, salary)
Here the dept_name attribute appears in both the relations. Here using common attributes in relation schema is one way of relating _____ relations.
a) Attributes of common
b) Tuple of common
c) Tuple of distinct
d) Attributes of distinct

Answer: a
Explanation: Here the relations are connected by the common attributes.

9. A domain is atomic if elements of the domain are considered to be _____ units.
a) Different
b) Indivisbile
c) Constant
d) Divisible

Answer: b

10. The tuples of the relations can be of _____ order.
a) Any
b) Same
c) Sorted
d) Constant

Answer: a
Explanation: The values only count. The order of the tuples does not matter.

1. Which one of the following is a set of one or more attributes taken collectively to uniquely identify a record?
a) Candidate key
b) Sub key
c) Super key
d) Foreign key

Answer: c
Explanation: Super key is the superset of all the keys in a relation.

2. Consider attributes ID, CITY and NAME. Which one of this can be considered as a super key?
a) NAME
b) ID
c) CITY
d) CITY, ID

Answer: b
Explanation: Here the id is the only attribute which can be taken as a key. Other attributes are not uniquely identified.

3. The subset of a super key is a candidate key under what condition?
a) No proper subset is a super key
b) All subsets are super keys
c) Subset is a super key
d) Each subset is a super key

Answer: a
Explanation: The subset of a set cannot be the same set. Candidate key is a set from a super key which cannot be the whole of the super set.

4. A _____ is a property of the entire relation, rather than of the individual tuples in which each tuple is unique.
a) Rows
b) Key
c) Attribute
d) Fields

Answer: b
Explanation: Key is the constraint which specifies uniqueness.

5. Which one of the following attribute can be taken as a primary key?
a) Name
b) Street
c) Id
d) Department

Answer: c
Explanation: The attributes name, street and department can repeat for some tuples. But the id attribute has to be unique. So it forms a primary key.

6. Which one of the following cannot be taken as a primary key?
a) Id
b) Register number
c) Dept_id
d) Street

Answer: d
Explanation: Street is the only attribute which can occur more than once.

7. An attribute in a relation is a foreign key if the _____ key from one relation is used as an attribute in that relation.
a) Candidate
b) Primary
c) Super
d) Sub

Answer: b
Explanation: The primary key has to be referred in the other relation to form a foreign key in that relation.

8. The relation with the attribute which is the primary key is referenced in another relation. The relation which has the attribute as a primary key is called _____
a) Referential relation
b) Referencing relation
c) Referenced relation
d) Referred relation

Answer: c
Explanation: The referenced relation is the table that contains the primary key being referenced.

9. The _____ is the one in which the primary key of one relation is used as a normal attribute in another relation.
a) Referential relation
b) Referencing relation
c) Referenced relation
d) Referred relation

Answer: b
Explanation: The referencing relation is the table that contains the foreign key.

10. A _____ integrity constraint requires that the values appearing in specified attributes of any tuple in the referencing relation also appear in specified attributes of at least one tuple in the referenced relation.
a) Referential
b) Referencing
c) Specific
d) Primary

Answer: a
Explanation: A relation, say r1, may include among its attributes the primary key of another relation, say r2. This attribute is called a foreign key from r1, referencing r2. The relation r1 is also called the referencing relation of the foreign key dependency, and r2 is called the referenced relation of the foreign key.

Relational Algebra - Database

1. Relational Algebra is a _____ query language that takes two relations as input and produces another relation as an output of the query.
a) Relational
b) Structural
c) Procedural
d) Fundamental

Answer: C

2. Which of the following is a fundamental operation in relational algebra?
a) Set intersection
b) Natural join
c) Assignment
d) None of the mentioned

Answer: d
Explanation: The fundamental operations are select, project, union, set difference, Cartesian product, and rename.

3. Which of the following is used to denote the selection operation in relational algebra?
a) Pi (Greek)
b) Sigma (Greek)
c) Lambda (Greek)
d) Omega (Greek)

Answer: b
Explanation: The select operation selects tuples that satisfy a given predicate.

4. For select operation the _____ appear in the subscript and the _____ argument appears in the paranthesis after the sigma.
a) Predicates, relation
b) Relation, Predicates
c) Operation, Predicates
d) Relation, Operation

Answer: a

5. The _____ operation, denoted by −, allows us to find tuples that are in one relation but are not in another.
a) Union
b) Set-difference
c) Difference
d) Intersection

Answer: b
Explanation: The expression r − s produces a relation containing those tuples in r but not in s.

6. Which is a unary operation:
a) Selection operation
b) Primitive operation

c) Projection operation
d) Generalized selection

Answer: d
Explanation: Generalization Selection takes only one argument for operation.

7. Which is a join condition contains an equality operator:
a) Equijoins
b) Cartesian
c) Natural
d) Left

Answer: a

8. In precedence of set operators, the expression is evaluated from
a) Left to left
b) Left to right
c) Right to left
d) From user specification

Answer: b
Explanation: The expression is evaluated from left to right according to the precedence.

9. Which of the following is not outer join?
a) Left outer join
b) Right outer join
c) Full outer join
d) All of the mentioned

Answer: d
Explanation: The FULL OUTER JOIN keyword combines the result of both LEFT and RIGHT joins.

10. The assignment operator is denoted by
a) ->
b) <-
c) =
d) ==

Answer: b
Explanation: The result of the expression to the right of the ← is assigned to the relation variable on the left of the ←.

Normalization

1. In the _____ normal form, a composite attribute is converted to individual attributes.
a) First
b) Second
c) Third
d) Fourth

Answer: a
Explanation: The first normal form is used to eliminate the duplicate information.

2. A table on the many side of a one to many or many to many relationship must:
a) Be in Second Normal Form (2NF)
b) Be in Third Normal Form (3NF)
c) Have a single attribute key
d) Have a composite key

Answer: d
Explanation: The relation in second normal form is also in first normal form and no partial dependencies on any column in primary key.

3. Tables in second normal form (2NF):
a) Eliminate all hidden dependencies
b) Eliminate the possibility of a insertion anomalies
c) Have a composite key
d) Have all non key fields depend on the whole primary key

Answer: a
Explanation: The relation in second normal form is also in first normal form and no partial dependencies on any column in primary key.

4. Which-one ofthe following statements about normal forms is FALSE?
a) BCNF is stricter than 3 NF
b) Lossless, dependency -preserving decomposition into 3 NF is always possible
c) Loss less, dependency – preserving decomposition into BCNF is always possible
d) Any relation with two attributes is BCNF

Answer: c
Explanation: We say that the decomposition is a lossless decomposition if there is no loss of information by replacing r (R) with two relation schemas r1(R1) andr2(R2).

5. Functional Dependencies are the types of constraints that are based on_____
a) Key
b) Key revisited
c) Superset key
d) None of the mentioned

Answer: a
Explanation: Key is the basic element needed for the constraints.

6. Which is a bottom-up approach to database design that design by examining the relationship between attributes:
a) Functional dependency
b) Database modeling
c) Normalization
d) Decomposition

Answer: c
Explanation: Normalisation is the process of removing redundancy and unwanted data.

7. Which forms simplifies and ensures that there are minimal data aggregates and repetitive groups:
a) 1NF
b) 2NF
c) 3NF
d) All of the mentioned

Answer: c
Explanation: The first normal form is used to eliminate the duplicate information.

8. Which forms has a relation that possesses data about an individual entity:
a) 2NF
b) 3NF
c) 4NF
d) 5NF

Answer: c
Explanation: A Table is in 4NF if and only if, for every one of its non-trivial multivalued dependencies X \twoheadrightarrow Y, X is a superkey—that is, X is either a candidate key or a superset thereof.

9. Which forms are based on the concept of functional dependency:
a) 1NF
b) 2NF
c) 3NF
d) 4NF

Answer: c
Explanation: The table is in 3NF if every non-prime attribute of R is non-transitively dependent (i.e. directly dependent) on every superkey of R.

10.Empdt1(empcode, name, street, city, state, pincode).

For any pincode, there is only one city and state. Also, for given street, city and state, there is just one pincode. In normalization terms, empdt1 is a relation in
a) 1 NF only
b) 2 NF and hence also in 1 NF
c) 3NF and hence also in 2NF and 1NF
d) BCNF and hence also in 3NF, 2NF and 1NF

Answer: b
Explanation: The relation in second normal form is also in first normal form and no partial dependencies on any column in primary key.

1. A relation is in _____ if an attribute of a composite key is dependent on an attribute of other composite key.
a) 2NF
b) 3NF
c) BCNF
d) 1NF

Answer: b
Explanation: A relation is in 3 NF if an attribute of a composite key is dependent on an attribute of other composite key. (If an attribute of a composite key is dependent on an attribute of other composite key then the relation is not in BCNF, hence it has to be decomposed.).

2. What are the desirable properties of a decomposition
a) Partition constraint
b) Dependency preservation
c) Redundancy
d) Security

Answer: b
Explanation: Lossless join and dependency preserving are the two goals of the decomposition.

3. R (A,B,C,D) is a relation. Which of the following does not have a lossless join dependency preserving BCNF decomposition?
a) A->B, B->CD
b) A->B, B->C, C->D

c) AB->C, C->AD
d) A->BCD

Answer: d
Explanation: This relation gives a relation without any loss in the values.

7. Which normal form is considered adequate for normal relational database design?
a) 2NF
b) 5NF
c) 4NF
d) 3NF

Answer: d
Explanation: A relational database table is often described as “normalized” if it is in the Third Normal Form because most of the 3NF tables are free of insertion, update, and deletion anomalies.

5. The algorithm that takes a set of dependencies and adds one schema at a time, instead of decomposing the initial schema repeatedly is
a) BCNF algorithm
b) 2NF algorithm
c) 3NF synthesis algorithm
d) 1NF algorithm

Answer: c
Explanation: The result is not uniquely defined, since a set of functional dependencies can have more than one canonical cover, and, further, in some cases, the result of the algorithm depends on the order in which it considers the dependencies in Fc.

6. The functional dependency can be tested easily on the materialized view, using the constraints _____.
a) Primary key
b) Null
c) Unique
d) Both Null and Unique

Answer: d
Explanation: Primary key contains both unique and not null constraints.

7. Which normal form is considered adequate for normal relational database design?
a) 2NF
b) 5NF

c) 4NF
d) 3NF

Answer: d
Explanation: A relational database table is often described as “normalized” if it is in the Third Normal Form because most of the 3NF tables are free of insertion, update, and deletion anomalies.

Transaction

1. A _____ consists of a sequence of query and/or update statements.
a) Transaction
b) Commit
c) Rollback
d) Flashback

Answer: a
Explanation: Transaction is a set of operation until commit.

2. Which of the following makes the transaction permanent in the database?
a) View
b) Commit
c) Rollback
d) Flashback

Answer: b
Explanation: Commit work commits the current transaction.

3. In order to undo the work of transaction after last commit which one should be used?
a) View
b) Commit
c) Rollback
d) Flashback

Answer: c
Explanation: Rollback work causes the current transaction to be rolled back; that is, it undoes all the updates performed by the SQL statements in the transaction.

4. Consider the following action:

TRANSACTION.....
Commit;

ROLLBACK;
What does Rollback do?
a) Undoes the transactions before commit
b) Clears all transactions
c) Redoes the transactions before commit
d) No action

Answer: d
Explanation: Once a transaction has executed commit work, its effects can no longer be undone by rollback work.

5. In case of any shut down during transaction before commit which of the following statement is done automatically?
a) View
b) Commit
c) Rollback
d) Flashback

Answer: c
Explanation: Once a transaction has executed commit work, its effects can no longer be undone by rollback work.

6. In order to maintain the consistency during transactions, database provides
a) Commit
b) Atomic
c) Flashback
d) Retain

Answer: b
Explanation: By atomic, either all the effects of the transaction are reflected in the database, or none are (after rollback).

7. Transaction processing is associated with everything below except
a) Conforming an action or triggering a response
b) Producing detail summary or exception report
c) Recording a business activity
d) Maintaining a data

Answer: a

8. A transaction completes its execution is said to be
a) Committed
b) Aborted

c) Rolled back
d) Failed

Answer: a
Explanation: A complete transaction always commits.

9. Which of the following is used to get back all the transactions back after rollback?
a) Commit
b) Rollback
c) Flashback
d) Redo

Answer: c
Explanation: None.

10. _____ will undo all statements up to commit?
a) Transaction
b) Flashback
c) Rollback
d) Abort

Answer: c
Explanation: Rollback will undo all statements up to commit. Flashback allows you to restore the database to a previous state, even after a COMMIT has been executed. Abort will terminate the operation.

1. In order to maintain transactional integrity and database consistency, what technology does a DBMS deploy?
a) Triggers
b) Pointers
c) Locks
d) Cursors

Answer: c
Explanation: Locks are used to maintain database consistency.

2. A lock that allows concurrent transactions to access different rows of the same table is known as a
a) Database-level lock
b) Table-level lock
c) Page-level lock
d) Row-level lock

Answer: d
Explanation: Locks are used to maintain database consistency.

3. Which of the following are introduced to reduce the overheads caused by the log-based recovery?
a) Checkpoints
b) Indices
c) Deadlocks
d) Locks

Answer: a
Explanation: Checkpoints are introduced to reduce overheads caused by the log-based recovery.

4. Which of the following protocols ensures conflict serializability and safety from deadlocks?
a) Two-phase locking protocol
b) Time-stamp ordering protocol
c) Graph based protocol
d) None of the mentioned

Answer: b
Explanation: Time-stamp ordering protocol ensures conflict serializability and safety from deadlocks.

5. Which of the following is the block that is not permitted to be written back to the disk?
a) Dead code
b) Read only
c) Pinned
d) Zapped

Answer: c
Explanation: A block that is not permitted to be written back to the disk is called pinned.

6. If transaction Ti gets an explicit lock on the file Fc in exclusive mode, then it has an _____ on all the records belonging to that file.
a) Explicit lock in exclusive mode
b) Implicit lock in shared mode
c) Explicit lock in shared mode
d) Implicit lock in exclusive mode

Answer: d
Explanation: If transaction Ti gets an explicit lock on the file Fc in exclusive mode, then it has an implicit lock in exclusive mode on all the records belonging to that file.

7. Which refers to a property of computer to run several operation simultaneously and possible as computers await response of each other
a) Concurrency
b) Deadlock
c) Backup
d) Recovery

Answer: a
Explanation: Concurrency is a property of systems in which several computations are executing simultaneously, and potentially interacting with each other.

8. All lock information is managed by a _____ which is responsible for assigning and policing the locks used by the transactions.
a) Scheduler
b) DBMS
c) Lock manager
d) Locking agent

Answer: c
Explanation: A distributed lock manager (DLM) provides distributed software applications with a means to synchronize their accesses to shared resources.

9. The ____ lock allows concurrent transactions to access the same row as long as they require the use of different fields within that row.
a) Table-level
b) Page-level
c) Row-level
d) Field-level

Answer: d
Explanation: Lock is limited to the attributes of the relation.

10. Which of the following is a procedure for acquiring the necessary locks for a transaction where all necessary locks are acquired before any are released?
a) Record controller
b) Exclusive lock
c) Authorization rule
d) Two phase lock

Answer: d
Explanation: Two-phase lock is a procedure for acquiring the necessary locks for a transaction where all necessary locks are acquired before any are released.

1. A system is in a _____ state if there exists a set of transactions such that every transaction in the set is waiting for another transaction in the set.
a) Idle
b) Waiting
c) Deadlock
d) Ready

Answer: c
Explanation: When one data item is waiting for another data item in a transaction then system is in deadlock.

2. The deadlock state can be changed back to stable state by using _____ statement.
a) Commit
b) Rollback
c) Savepoint
d) Deadlock

Answer: b
Explanation: Rollback is used to rollback to the point before lock is obtained.

3. What are the ways of dealing with deadlock?
a) Deadlock prevention
b) Deadlock recovery
c) Deadlock detection
d) All of the mentioned

Answer: d
Explanation: Deadlock prevention is also called as deadlock recovery. Prevention is commonly used if the probability that the system would enter a deadlock state is relatively high; otherwise, detection and recovery are more efficient.

4. When transaction Ti requests a data item currently held by Tj, Ti is allowed to wait only if it has a timestamp smaller than that of Tj (that is, Ti is older than Tj). Otherwise, Ti is rolled back (dies). This is
a) Wait-die
b) Wait-wound
c) Wound-wait
d) Wait

Answer: a
Explanation: The wait–die scheme is a non-preemptive technique.

5. When transaction Ti requests a data item currently held by Tj, Ti is allowed to wait only if it has a timestamp larger than that of Tj (that is, Ti is younger than Tj). Otherwise, Tj is rolled back (Tj is wounded by Ti). This is
a) Wait-die
b) Wait-wound
c) Wound-wait
d) Wait

Answer: c
Explanation: The wound–wait scheme is a preemptive technique. It is a counterpart to the wait–die scheme.

6. The situation where the lock waits only for a specified amount of time for another lock to be released is
a) Lock timeout
b) Wait-wound
c) Timeout
d) Wait

Answer: a
Explanation: The timeout scheme is particularly easy to implement, and works well if transactions are short and if longwaits are likely to be due to deadlocks.

7. The deadlock in a set of a transaction can be determined by
a) Read-only graph
b) Wait graph
c) Wait-for graph
d) All of the mentioned

Answer: a
Explanation: Each transaction involved in the cycle is said to be deadlocked.

8. A deadlock exists in the system if and only if the wait-for graph contains a _____
a) Cycle
b) Direction
c) Bi-direction
d) Rotation

Answer: a
Explanation: Each transaction involved in the cycle is said to be deadlocked.

9. Selecting the victim to be rollbacked to the previous state is determined by the minimum cost. The factors determining cost of rollback is

a) How long the transaction has computed, and how much longer the transaction will compute before it completes its designated task
b) How many data items the transaction has used
c) How many more data items the transaction needs for it to complete
d) All of the mentioned

Answer: d
Explanation: We should roll back those transactions that will incur the minimum cost.

10. _____ rollback requires the system to maintain additional information about the state of all the running transactions.
a) Total
b) Partial
c) Time
d) Commit

Answer: b
Explanation: In total rollback abort the transaction and then restart it.

Computer Network

1. How many layers are present in the Internet protocol stack (TCP/IP model)?
a) 5
b) 7
c) 6
d) 10

Answer: a
Explanation: There are five layers in the Internet Protocol stack. The five layers in Internet Protocol stack is Application, Transport, Network, Data link and Physical layer. The internet protocol stack model is also called the TCP/IP model and it's used in modern Internet Communication.

2. The number of layers in ISO OSI reference model is _____
a) 5
b) 7
c) 6
d) 10

Answer: b
Explanation: The seven layers in ISO OSI reference model is Application, Presentation, Session, Transport, Network, Data link and Physical layer. OSI stands for Open System Interconnect and it is a generalized model.

3. Which of the following layers is an addition to OSI model when compared with TCP IP model?
a) Application layer
b) Presentation layer
c) Session layer
d) Session and Presentation layer

Answer: d
Explanation: The only difference between OSI model and TCP/IP model is that the functions of Presentation and Session layer in the OSI model are handled by the transport layer itself in TCP/IP. OSI is a generalized model and TCP/IP is an application specific model.

4. Application layer is implemented in _____
a) End system
b) NIC
c) Ethernet
d) Packet transport

Answer: a
Explanation: Not only application layer, but presentation layer, session layer and transport layer are also implemented in the end system. The layers below are implemented outside the end system, for example, the network layer is implemented on the routers and the physical layer is implemented for the medium.

5. Transport layer is implemented in _____
a) End system
b) NIC
c) Ethernet
d) Signal transmission

Answer: a
Explanation: Application, Presentation, Session and Transport layer are implemented in the end system. The transport layer handles the process to process delivery of the packet through ports.

6. The functionalities of the presentation layer include _____
a) Data compression
b) Data encryption
c) Data description
d) All of the mentioned

Answer: d
Explanation: Some functions of the presentation layer include character-code translation, data conversion, data encryption and decryption, and data translation. It connects the application layer

with the layers below converting the human readable text and media to machine readable format and vice-versa.

7. Delimiting and synchronization of data exchange is provided by _____
a) Application layer
b) Session layer
c) Transport layer
d) Link layer

Answer: b
Explanation: The session layer provides the mechanism for opening, closing and managing a session between end-user application processes. The session layer 5 is responsible for establishing managing synchronizing and terminating sessions. In TCP/IP protocol stack, the functions of the session layer are handled by the transport layer itself and thus the session layer is missing from the TCP/IP model.

8. In OSI model, when data is sent from device A to device B, the 5th layer to receive data at B is _____
a) Application layer
b) Transport layer
c) Link layer
d) Session layer

Answer: d
Explanation: In OSI reference model, the fifth layer is Session layer. Session layer provides the mechanism for opening, closing and managing a session between end-user application processes. In TCP/IP protocol stack, the functions of the session layer are handled by the transport layer itself and thus the session layer is missing from the TCP/IP model.

9. In TCP IP Model, when data is sent from device A to device B, the 5th layer to receive data at B is _____
a) Application layer
b) Transport layer
c) Link layer
d) Session layer

Answer: a
Explanation: In TCP/IP model, the fifth layer is application layer. When data is sent from device A to device B, the 5th layer to receive data at B is application layer. Application layer provides the interface between applications and the network. The user interacts with only this layer.

10. In the OSI model, as a data packet moves from the lower to the upper layers, headers are _____

a) Added
b) Removed
c) Rearranged
d) Randomized

Answer: b
Explanation: In OSI reference model, when data packet moves from lower layers to higher layer, headers get removed. Whereas when the data packet moves from higher layer to lower layers, headers are added. These headers contain the essential control information for the protocols used on the specific layer.

11. Which of the following statements can be associated with OSI model?
a) A structured way to discuss and easier update system components
b) One layer may duplicate lower layer functionality
c) Functionality at one layer no way requires information from another layer
d) It is an application specific network model

Answer: a
Explanation: The OSI model provides a standardized framework for network communication by dividing it into layers. This layered approach simplifies troubleshooting, enables modular updates, and ensures interoperability between different network devices and protocols.

1. OSI stands for _____
a) open system interconnection
b) operating system interface
c) optical service implementation
d) open service Internet

Answer: a
Explanation: OSI is the abbreviation for Open System Interconnection. OSI model provides a structured plan on how applications communicate over a network, which also helps us to have a structured plan for troubleshooting. It is recognized by the ISO as the generalized model for computer network i.e. it can be modified to design any kind of computer network.

2. The number of layers in ISO OSI reference model is _____
a) 4
b) 5
c) 6
d) 7

Answer: d
Explanation: In OSI reference model, there are 7 layers namely Application, Presentation, Session, Transport, Network, Data Link and Physical layer. Each layer uses a protocol to perform its

designated function, for example, the data link layer uses error detection protocols for error control functions.

3. TCP/IP model does not have _____ layer but OSI model have this layer.
a) session layer
b) transport layer
c) application layer
d) network layer

Answer: a
Explanation: In OSI reference model, there are two layers which are not present in TCP/IP model. They are Presentation and Session layer. The functions of Presentation and Session layer in the OSI model are handled by the transport layer itself in TCP/IP.

4. Which layer is used to link the network support layers and user support layers?
a) session layer
b) data link layer
c) transport layer
d) network layer

Answer: c
Explanation: Physical, data link and network layers are network support layers and session, presentation and application layers are user support layers. The transport layer links these layers by segmenting and rearranging the data. It uses protocols like TCP and UDP.

5. Which address is used on the internet for employing the TCP/IP protocols?
a) physical address and logical address
b) port address
c) specific address
d) all of the mentioned

Answer: d
Explanation: The physical, logical, port and specific addresses are used in TCP/IP protocol. All the addressing schemes, that is physical (MAC) and logical address, port address and specific address are employed in both TCP/IP model and OSI model. In TCP/IP, the addresses are more focused on the internet implementation of these addresses.

6. TCP/IP model was developed _____ the OSI model.
a) prior to
b) after
c) simultaneous to
d) with no link to

Answer: a
Explanation: Several TCP/IP prototypes were developed at multiple research centers between 1978 and 1983, whereas OSI reference model was developed in the year 1984. TCP/IP was developed with the intention to create a model for the Internet while OSI was intended to be a general network model.

7. Which layer is responsible for process to process delivery in a general network model?
a) network layer
b) transport layer
c) session layer
d) data link layer

Answer: b
Explanation: The role of Transport layer (Layer 4) is to establish a logical end to end connection between two systems in a network. The protocols used in Transport layer is TCP and UDP. The transport layer is responsible for segmentation of the data. It uses ports for the implementation of process-to-process delivery.

8. Which address is used to identify a process on a host by the transport layer?
a) physical address
b) logical address
c) port address
d) specific address

Answer: c
Explanation: A port number is a way to identify a specific process to which an Internet or other network message is to be forwarded when it arrives at a server. Some examples of port numbers are port 20 which is used for FTP data, port 22 which is used for SSH remote login ,and port 23 which is used for TELNET.

9. Which layer provides the services to user?
a) application layer
b) session layer
c) presentation layer
d) physical layer

Answer: a
Explanation: In networking, a user mainly interacts with application layer to create and send information to other computer or network. Application layer provides the interface between applications and the network. It is the top-most layer in both the TCP/IP and the OSI model.

10. Transmission data rate is decided by _____
a) network layer

b) physical layer
c) data link layer
d) transport layer

Answer: b
Explanation: Physical layer is a layer 1 device which deals with network cables or the standards in use like connectors, pins, electric current used etc. Basically the transmission speed is determined by the cables and connectors used. Hence it is physical layer that determines the transmission speed in network. Some of the cables used for high speed data transmission are optical fiber cables and twisted pair cables.

Physical Model

1. The physical layer is concerned with _____
a) bit-by-bit delivery
b) process to process delivery
c) application to application delivery
d) port to port delivery

Answer: a
Explanation: Physical layer deals with bit to bit delivery in networking. The data unit in the physical layer is bits. Process to process delivery or the port to port delivery is dealt in the transport layer. The various transmission mediums aid the physical layer in performing its functions.

2. Which transmission media provides the highest transmission speed in a network?
a) coaxial cable
b) twisted pair cable
c) optical fiber
d) electrical cable

Answer: c
Explanation: Fiber optics is considered to have the highest transmission speed among the all mentioned above. The fiber optics transmission runs at 1000Mb/s. It is called as 1000Base-Lx whereas IEEE standard for it is 802.3z. It is popularly used for modern day network connections due to its high transmission rate.

3. Bits can be sent over guided and unguided media as analog signal by _____
a) digital modulation
b) amplitude modulation
c) frequency modulation
d) phase modulation

Answer: a
Explanation: In analog modulation, digital low frequency baseband signal (digital bit stream) is transmitted over a higher frequency. Whereas in digital modulation the only difference is that the base band signal is of discrete amplitude level. The bits are represented by only two frequency levels, one for high and one for low.

4. The portion of physical layer that interfaces with the media access control sublayer is called _____
a) physical signalling sublayer
b) physical data sublayer
c) physical address sublayer
d) physical transport sublayer

Answer: a
Explanation: The portion of physical layer that interfaces with the medium access control sublayer is Physical Signaling Sublayer. The main function of this layer is character encoding, reception, decoding and performs optional isolation functions. It handles which media connection the signal should be forwarded to physically.

5. The physical layer provides _____
a) mechanical specifications of electrical connectors and cables
b) electrical specification of transmission line signal level
c) specification for IR over optical fiber
d) all of the mentioned

Answer: d
Explanation: Anything dealing with a network cable or the standards in use – including pins, connectors and the electric current used is dealt in the physical layer (Layer 1). Physical layer deals with bit to bit delivery of the data aided by the various transmission mediums.

6. In asynchronous serial communication the physical layer provides _____
a) start and stop signalling
b) flow control
c) both start & stop signalling and flow control
d) only start signalling

Answer: c
Explanation: In asynchronous serial communication, the communication is not synchronized by clock signal. Instead of a start and stop signaling and flow control method is followed. Unlike asynchronous serial communication, in synchronous serial communication a clock signal is used for communication, so the start and stop method is not really required.

7. The physical layer is responsible for _____
a) line coding
b) channel coding
c) modulation
d) all of the mentioned

Answer: d
Explanation: The physical layer is responsible for line coding, channel coding and modulation that is needed for the transmission of the information. The physical configuration including pins, connectors and the electric current used is dealt in the physical layer based on the requirement of the network application.

8. The physical layer translates logical communication requests from the _____ into hardware specific operations.
a) data link layer
b) network layer
c) trasnport layer
d) application layer

Answer: a
Explanation: Physical layer accepts data or information from the data link layer and converts it into hardware specific operations so as to transfer the message through physical cables. Some examples of the cables used are optical fiber cables, twisted pair cables and co-axial cables.

9. A single channel is shared by multiple signals by _____
a) analog modulation
b) digital modulation
c) multiplexing
d) phase modulation

Answer: c
Explanation: In communication and computer networks, the main goal is to share a scarce resource. This is done by multiplexing, where multiple analog or digital signals are combined into one signal over a shared medium. The multiple kinds of signals are designated by the transport layer which is the layer present on a higher level than the physical layer.

10. Wireless transmission of signals can be done via _____
a) radio waves
b) microwaves
c) infrared
d) all of the mentioned

Answer: d
Explanation: Wireless transmission is carried out by radio waves, microwaves and IR waves. These waves range from 3 Khz to above 300 Ghz and are more suitable for wireless transmission. Radio waves can penetrate through walls and are used in radio communications, microwaves and infrared (IR) waves cannot penetrate through walls and are used for satellite communications and device communications respectively.

Data Link Layer

1. The data link layer takes the packets from _____ and encapsulates them into frames for transmission.
a) network layer
b) physical layer
c) transport layer
d) application layer

Answer: a
Explanation: In computer networks, the data from application layer is sent to transport layer and is converted to segments. These segments are then transferred to the network layer and these are called packets. These packets are then sent to data link layer where they are encapsulated into frames. These frames are then transferred to physical layer where the frames are converted to bits. Error control and flow control data is inserted in the frames at the data link layer.

2. Which of the following tasks is not done by data link layer?
a) framing
b) error control
c) flow control
d) channel coding

Answer: d
Explanation: Channel coding is the function of physical layer. Data link layer mainly deals with framing, error control and flow control. Data link layer is the layer where the packets are encapsulated into frames.

3. Which sublayer of the data link layer performs data link functions that depend upon the type of medium?
a) logical link control sublayer
b) media access control sublayer
c) network interface control sublayer
d) error control sublayer

Answer: b
Explanation: Media access control (MAC) deals with transmission of data packets to and from the

network-interface card, and also to and from another remotely shared channel. The MAC sublayer also prevents collision using protocols like CSMA/CD.

4. Header of a frame generally contains _____
a) synchronization bytes
b) addresses
c) frame identifier
d) all of the mentioned

Answer: d
Explanation: In a frame, the header is a part of the data that contains all the required information about the transmission of the file. It contains information like synchronization bytes, addresses, frame identifier etc. It also contains error control information for reducing the errors in the transmitted frames.

5. Automatic repeat request error management mechanism is provided by _____
a) logical link control sublayer
b) media access control sublayer
c) network interface control sublayer
d) application access control sublayer

Answer: a
Explanation: The logical link control is a sublayer of data link layer whose main function is to manage traffic, flow and error control. The automatic repeat request error management mechanism is provided by the LLC when an error is found in the received frame at the receiver's end to inform the sender to re-send the frame.

6. When 2 or more bits in a data unit has been changed during the transmission, the error is called _____
a) random error
b) burst error
c) inverted error
d) double error

Answer: b
Explanation: When a single bit error occurs in a data, it is called single bit error. When more than a single bit of data is corrupted or has error, it is called burst error. If a single bit error occurs, the bit can be simply repaired by inverting it, but in case of a burst error, the sender has to send the frame again.

7. CRC stands for _____
a) cyclic redundancy check
b) code repeat check

c) code redundancy check
d) cyclic repeat check

Answer: a
Explanation: Cyclic redundancy check is a code that is added to a data which helps us to identify any error that occurred during the transmission of the data. CRC is only able to detect errors, not correct them. CRC is inserted in the frame trailer.

8. Which of the following is a data link protocol?
a) ethernet
b) point to point protocol
c) hdlc
d) all of the mentioned

Answer: d
Explanation: There are many data link layer protocols. Some of them are SDLC (synchronous data link protocol), HDLC (High level data link control), SLIP (serial line interface protocol), PPP (Point to point protocol) etc. These protocols are used to provide the logical link control function of the Data Link Layer.

9. Which of the following is the multiple access protocol for channel access control?
a) CSMA/CD
b) CSMA/CA
c) Both CSMA/CD & CSMA/CA
d) HDLC

Answer: c
Explanation: In CSMA/CD, it deals with detection of collision after collision has occurred, whereas CSMA/CA deals with preventing collision. CSMA/CD is abbreviation for Carrier Sensing Multiple Access/Collision detection. CSMA/CA is abbreviation for Carrier Sensing Multiple Access/Collision Avoidance. These protocols are used for efficient multiple channel access.

10. The technique of temporarily delaying outgoing acknowledgements so that they can be hooked onto the next outgoing data frame is called _____
a) piggybacking
b) cyclic redundancy check
c) fletcher’s checksum
d) parity check

Answer: a
Explanation: Piggybacking is a technique in which the acknowledgment is temporarily delayed so as to be hooked with the next outgoing data frame. It saves a lot of channel bandwidth as in non-piggybacking system, some bandwidth is reserved for acknowledgement.

Network Layer

1. The network layer is concerned with _____ of data.
a) bits
b) frames
c) packets
d) bytes

Answer: c
Explanation: In computer networks, the data from the application layer is sent to the transport layer and is converted to segments. These segments are then transferred to the network layer and these are called packets. These packets are then sent to data link layer where they are encapsulated into frames. These frames are then transferred to physical layer where the frames are converted to bits.

2. Which one of the following is not a function of network layer?
a) routing
b) inter-networking
c) congestion control
d) error control

Answer: d
Explanation: In the OSI model, network layer is the third layer and it provides data routing paths for network communications. Error control is a function of the data link layer and the transport layer.

3. A 4 byte IP address consists of _____
a) only network address
b) only host address
c) network address & host address
d) network address & MAC address

Answer: c
Explanation: An ip address which is 32 bits long, that means it is of 4 bytes and is composed of a network and host portion and it depends on address class. The size of the host address and network address depends upon the class of the address in classful IP addressing.

4. In virtual circuit network each packet contains _____
a) full source and destination address
b) a short VC number
c) only source address
d) only destination address

Answer: b
Explanation: A short VC number also called as VCID (virtual circuit identifier) is a type of identifier

which is used to distinguish between several virtual circuits in a connection oriented circuit switched network. Each virtual circuit is used to transfer data over a larger packet switched network.

5. Which of the following routing algorithms can be used for network layer design?
a) shortest path algorithm
b) distance vector routing
c) link state routing
d) all of the mentioned

Answer: d
Explanation: The routing algorithm is what decides where a packet should go next. There are several routing techniques like shortest path algorithm, static and dynamic routing, decentralized routing, distance vector routing, link state routing, Hierarchical routing etc. The routing algorithms go hand in hand with the operations of all the routers in the networks. The routers are the main participants in these algorithms.

6. Which of the following is not correct in relation to multi-destination routing?
a) is same as broadcast routing
b) contains the list of all destinations
c) data is not sent by packets
d) there are multiple receivers

Answer: c
Explanation: In multi-destination routing, there is more than one receiver and the route for each destination which is contained in a list of destinations is to be found by the routing algorithm. Multi-destination routing is also used in broadcasting.

7. A subset of a network that includes all the routers but contains no loops is called
a) spanning tree
b) spider structure
c) spider tree
d) special tree

Answer: a
Explanation: Spanning tree protocol (STP) is a network protocol that creates a loop free logical topology for ethernet networks. It is a layer 2 protocol that runs on bridges and switches. The main purpose of STP is to ensure that you do not create loops when you have redundant paths in your network.

8. Which one of the following algorithm is not used for congestion control?
a) traffic aware routing
b) admission control

c) load shedding
d) routing information protocol

Answer: d
Explanation: The Routing Information Protocol (RIP) is used by the network layer for the function of dynamic routing. Congestion control focuses on the flow of the traffic in the network and uses algorithms like traffic aware routing, admission control and load shedding to deal with congestion.

9. The network layer protocol for internet is _____
a) ethernet
b) internet protocol
c) hypertext transfer protocol
d) file transfer protocol

Answer: b
Explanation: There are several protocols used in Network layer. Some of them are IP, ICMP, CLNP, ARP, IPX, HRSP etc. Hypertext transfer protocol is for application layer and ethernet protocol is for data link layer.

10. ICMP is primarily used for _____
a) error and diagnostic functions
b) addressing
c) forwarding
d) routing

Answer: a
Explanation: ICMP abbreviation for Internet Control Message Protocol is used by networking devices to send error messages and operational information indicating a host or router cannot be reached. ICMP operates over the IP packet to provide error reporting functionality as IP by itself cannot report errors.

Transport Layer

1. Transport layer aggregates data from different applications into a single stream before passing it to _____
a) network layer
b) data link layer
c) application layer
d) physical layer

Answer: a
Explanation: The flow of data in the OSI model flows in following manner Application -> Presentation

-> Session -> Transport -> Network -> Data Link -> Physical. Each and every layer has its own set of functions and protocols to ensure efficient network performance.

2. Which of the following are transport layer protocols used in networking?
a) TCP and FTP
b) UDP and HTTP
c) TCP and UDP
d) HTTP and FTP

Answer: c
Explanation: Both TCP and UDP are transport layer protocol in networking. TCP is an abbreviation for Transmission Control Protocol and UDP is an abbreviation for User Datagram Protocol. TCP is connection oriented whereas UDP is connectionless.

3. User datagram protocol is called connectionless because _____
a) all UDP packets are treated independently by transport layer
b) it sends data as a stream of related packets
c) it is received in the same order as sent order
d) it sends data very quickly

Answer: a
Explanation: UDP is an alternative for TCP and it is used for those purposes where speed matters most whereas loss of data is not a problem. UDP is connectionless whereas TCP is connection oriented.

4. Transmission control protocol _____
a) is a connection-oriented protocol
b) uses a three way handshake to establish a connection
c) receives data from application as a single stream
d) all of the mentioned

Answer: d
Explanation: TCP provides reliable and ordered delivery of a stream of bytes between hosts communicating via an IP network. Major internet applications like www, email, file transfer etc rely on TCP. TCP is connection oriented and it is optimized for accurate delivery rather than timely delivery.

5. An endpoint of an inter-process communication flow across a computer network is called _____
a) socket
b) pipe
c) port
d) machine

Answer: a
Explanation: Socket is one end point in a two way communication link in the network. TCP layer can identify the application that data is destined to be sent by using the port number that is bound to socket.

6. Socket-style API for windows is called _____
a) wsock
b) winsock
c) wins
d) sockwi

Answer: b
Explanation: Winsock is a programming interface which deals with input output requests for internet applications in windows OS. It defines how windows network software should access network services.

7. Which one of the following is a version of UDP with congestion control?
a) datagram congestion control protocol
b) stream control transmission protocol
c) structured stream transport
d) user congestion control protocol

Answer: a
Explanation: The datagram congestion control is a transport layer protocol which deals with reliable connection setup, teardown, congestion control, explicit congestion notification, and feature negotiation. It is used in modern day systems where there are really high chances of congestion. The protocol was last updated in the year 2008.

8. A _____ is a TCP name for a transport service access point.
a) port
b) pipe
c) node
d) protocol

Answer: a
Explanation: Just as the IP address identifies the computer, the network port identifies the application or service running on the computer. A port number is 16 bits. The combination of IP address preceded with the port number is called the socket address.

9. Transport layer protocols deals with _____
a) application to application communication
b) process to process communication

c) node to node communication
d) man to man communication

Answer: b
Explanation: Transport layer is 4th layer in TCP/IP model and OSI reference model. It deals with logical communication between process. It is responsible for delivering a message between network host.

10. Which of the following is a transport layer protocol?
a) stream control transmission protocol
b) internet control message protocol
c) neighbor discovery protocol
d) dynamic host configuration protocol

Answer: a
Explanation: The Stream Control Transmission Protocol (SCTP) is a transport layer protocol used in networking system where streams of data are to be continuously transmitted between two connected network nodes. Some of the other transport layer protocols are RDP, RUDP, TCP, DCCP, UDP etc.

TCP/IP

1. What layer in the TCP/IP stack is equivalent to the Transport layer of the OSI model?
a) Application
b) Host to host
c) Internet
d) Network Access

Answer: b
Explanation: The four layers of the TCP/IP stack (also called the DoD model) are Application/Process, Host-to-Host, Internet, and Network Access. The Host-to-Host layer is equivalent to the Transport layer of the OSI model.

2. You want to implement a mechanism that automates the IP configuration, including IP address, subnet mask, default gateway, and DNS information. Which protocol will you use to accomplish this?
a) SMTP
b) SNMP
c) DHCP
d) ARP

Answer: c
Explanation: Dynamic Host Configuration Protocol (DHCP) is used to provide IP information to hosts on your network. DHCP can provide a lot of information, but the most common is the IP address, subnet mask, default gateway, and DNS information.

3. The DoD model (also called the TCP/IP stack) has four layers. Which layer of the DoD model is equivalent to the Network layer of the OSI model?
a) Application
b) Host to Host
c) Internet
d) Network Access

Answer: c
Explanation: The four layers of the DoD model are Application/Process, Host-to-Host, Internet, and Network Access. The Internet layer is equivalent to the Network layer of the OSI model.

4. Which of the following protocols uses both TCP and UDP?
a) FTP
b) SMTP
c) Telnet
d) DNS

Answer: d
Explanation: DNS and some other services work on both TCP and the UDP protocols. DNS uses TCP for zone exchanges between servers and UDP when a client is trying to resolve a hostname to an IP address.

5. Length of Port address in TCP/IP is _____
a) 4bit long
b) 16bit long
c) 32bit long
d) 8 bit long

Answer: b
Explanation: TCP and UDP port numbers are 16 bits in length. So, valid port numbers can theoretically take on values from 0 to 65,535. These values are divided into ranges for different purposes, with certain ports reserved for particular uses.

6. TCP/IP layer is equivalent to combined Session, Presentation and _____
a) Network layer
b) Application layer
c) Transport layer
d) Physical layer

Answer: b
Explanation: TCP/IP network model is a hierarchical protocol made up of interactive modules, each of which provides a specific functionality; however, the modules are not necessarily interdependent. It is equivalent to combined session, presentation and application layer.

7. How many levels of addressing is provided in TCP/IP protocol?
a) One
b) Two
c) Three
d) Four

Answer: d
Explanation: Four levels of addresses are used in the internet employing the TCP/IP protocols. They are physical (link) addresses, logical (IP) addresses, port addresses, and specific addresses.

8. Virtual terminal protocol is an example of _____
a) Network layer
b) Application layer
c) Transport layer
d) Physical layer

Answer: b
Explanation: In open systems, a virtual terminal (VT) is an application service. It allows host terminals on a multi-user network to interact with other hosts regardless of terminal type and characteristics.

9. TCP/IP is related to _____
a) ARPANET
b) OSI
c) DECNET
d) ALOHA

Answer: a
Explanation: In 1983, TCP/IP protocols replaced NCP (Network Control Program) as the ARPANET's principal protocol. And ARPANET then became one component of the early Internet. The starting point for host-to-host communication on the ARPANET in 1969 was the 1822 protocol, which defined the transmission of messages to an IMP.

10. A device operating at network layer is called _____
a) Router
b) Equalizer
c) Bridge
d) Repeater

Answer: a
Explanation: A router is a networking device that forwards data packets between computer networks. Routers perform the traffic directing functions on the Internet. It supports different network layer

transmission standards. Each network interface is used to enable data packets to be forwarded from one transmission system to another.

11. A device operating at physical layer is called _____
a) Router
b) Equalizer
c) Bridge
d) Repeater

Answer: d
Explanation: A repeater connects two segments of your network cable. It retimes and regenerates the signals to proper amplitudes and sends them to the other segments. Repeaters work only at the physical layer of the OSI network model.

Congestion Control

1. Two broad categories of congestion control are
a) Open-loop and Closed-loop
b) Open-control and Closed-control
c) Active control and Passive control
d) Active loop and Passive loop

Answer: a
Explanation: Open loop congestion control techniques are used to prevent congestion before it even happens by enforcing certain policies. Closed loop congestion control techniques are used to treat congestion after it has happened.

2. In open-loop control, policies are applied to _____
a) Remove after congestion occurs
b) Remove after sometime
c) Prevent before congestion occurs
d) Prevent before sending packets

Answer: c
Explanation: Open loop congestion control techniques are used to prevent congestion before it even happens by enforcing certain policies. Retransmission policy, window policy and acknowledgement policy are some policies that might be enforced.

3. Retransmission of packets must not be done when _____
a) Packet is lost
b) Packet is corrupted
c) Packet is needed
d) Packet is error-free

Answer: d
Explanation: Retransmission refers to the sender having to resend the packet to the receiver. It needs to be done only when some anomaly occurs with the packet like when the packet is lost or corrupted.

4. In Go-Back-N window, when the timer of the packet times out, several packets have to be resent even some may have arrived safe. Whereas in Selective Repeat window, the sender resends _____
a) Packet which are not lost
b) Only those packets which are lost or corrupted
c) Packet from starting
d) All the packets

Answer: b
Explanation: In Selective Repeat, the sender side uses a searching algorithm to find the packets which need to be retransmitted based on the negative acknowledgements received and then resends only those packets thus saving bandwidth.

5. Discarding policy is mainly done by _____
a) Sender
b) Receiver
c) Router
d) Switch

Answer: c
Explanation: The discarding policy adopted by the routers mainly states that the routers discard sensitive or corrupted packets that it receives, thus controlling the integrity of the packet flow. The discarding policy is adopted as an open loop congestion control technique.

6. Closed-Loop control mechanisms try to _____
a) Remove after congestion occurs
b) Remove after sometime
c) Prevent before congestion occurs
d) Prevent before sending packets

Answer: a
Explanation: In closed loop congestion control, methods are implemented to remove congestion after it occurs. Some of the methods used are backpressure and choke packet.

7. The technique in which a congested node stops receiving data from the immediate upstream node or nodes is called as _____
a) Admission policy
b) Backpressure

c) Forward signaling
d) Backward signaling

Answer: b
Explanation: In this closed loop congestion control technique, the congested node propagates in the opposite direction of the data flow to inform the predecessor node to reduce the flow of packets. This is why this technique is called a node-to-node congestion control technique.

8. Backpressure technique can be applied only to _____
a) Congestion networks
b) Closed circuit networks
c) Open circuit networks
d) Virtual circuit networks

Answer: d
Explanation: In Virtual circuit networks, each node knows the upstream node from which a flow data is coming. So, it makes possible for the congested node to track the source of the congestion and then inform that node to reduce the flow to remove congestion.

9. The packet sent by a node to the source to inform it of congestion is called _____
a) Explicit
b) Discard
c) Choke
d) Backpressure

Answer: c
Explanation: Choke packet is sent by a node to the source to inform it of congestion. Two choke packet techniques can be used for the operation called hop-by-hop choke packet and source choke packet.

10. In the slow-start algorithm, the size of the congestion window increases _____ until it reaches a threshold.
a) exponentially
b) additively
c) multiplicatively
d) suddenly

Answer: a
Explanation: In slow-start algorithm, the size of the congestion window increases exponentially until it reaches a threshold. When it reaches the threshold, it stops increasing and continues sending packets through the threshold window thus preventing congestion.

11. In the congestion avoidance algorithm, the size of the congestion window increases _____ until congestion is detected.
a) exponentially
b) additively
c) multiplicatively
d) suddenly

Answer: b
Explanation: In the congestion avoidance algorithm, the size of the congestion window increases additively until congestion is detected. Once congestion is detected, the size of congestion window is decreased once and then the packets are transmitted to achieve congestion avoidance.

IPv4

1. Which of the following is not applicable for IP?
a) Error reporting
b) Handle addressing conventions
c) Datagram format
d) Packet handling conventions

Answer: a
Explanation: The Internet Protocol is the networking protocol which establishes the internet by relaying datagrams across network boundaries. ICMP is a supporting protocol for IP which handles the Error Reporting functionality.

2. Which of the following field in IPv4 datagram is not related to fragmentation?
a) Flags
b) Offset
c) TOS
d) Identifier

Answer: c}
Explanation: TOS-type of service identifies the type of packets. It is not related to fragmentation but is used to request specific treatment such as high throughput, high reliability or low latency for the IP packet depending upon the type of service it belongs to.

3. The TTL field has value 10. How many routers (max) can process this datagram?
a) 11
b) 5
c) 10
d) 1

Answer: c
Explanation: TTL stands for Time to Live. This field specifies the life of the IP packet based on the number of hops it makes (Number of routers it goes through). TTL field is decremented by one each time the datagram is processed by a router. When the value is 0, the packet is automatically destroyed.

4. If the value in protocol field is 17, the transport layer protocol used is _____
a) TCP
b) UDP
c) ICMP
d) IGMP

Answer: b
Explanation: The protocol field enables the demultiplexing feature so that the IP protocol can be used to carry payloads of more than one protocol type. Its most used values are 17 and 6 for UDP and TCP respectively. ICMP and IGMP are network layer protocols.

5. The data field cannot carry which of the following?
a) TCP segment
b) UDP segment
c) ICMP messages
d) SMTP messages

Answer: d
Explanation: Data field usually has transport layer segments, but it can also carry ICMP messages. SMTP is an application layer protocol. First it must go through the transport layer to be converted into TCP segments and then it can be inserted into IP packets.

6. What should be the flag value to indicate the last fragment?
a) 0
b) 1
c) TTl value
d) Protocol field value

Answer: a
Explanation: The Flag field in the IP header is used to control and identify the fragments. It contains three bits: reserved, don’t fragment and more fragments. If the more fragments bit is 0, it means that the fragment is the last fragment.

7. Which of these is not applicable for IP protocol?
a) is connectionless
b) offer reliable service

c) offer unreliable service
d) does not offer error reporting

Answer: b
Explanation: IP does not provide reliable delivery service for the data. It's dependent upon the transport layer protocols like TCP to offer reliability.

8. Which of the following demerits does Fragmentation have?
a) complicates routers
b) open to DOS attack
c) overlapping of fragments.
d) all of the mentioned

Answer: d
Explanation: Fragmentation makes the implementation of the IP protocol complex and can also be exploited by attackers to create a DOS attack such as a teardrop attack. Fragmentation won't be required if the transport layer protocols perform wise segmentation.

9. Which field helps to check rearrangement of the fragments?
a) offset
b) flag
c) ttl
d) identifer

Answer: a
Explanation: The Fragment Offset field specifies where the fragment fits in the original datagram. The offset of the first fragment will always be 0. The size of the field (13 bits) is 3-bits shorter than the size of the total length field (16 bits).

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4. In classless addressing, there are no classes but addresses are still granted in _____
a) IPs
b) Blocks
c) Codes
d) Sizes

Answer: b
Explanation: In classless addressing, there are no classes but addresses are still granted in blocks. The total number of addresses in a block of classless IP addresses = 2(32 – CIDR_value).

5. In IPv4 Addresses, classful addressing is replaced with _____
a) Classless Addressing
b) Classful Addressing
c) Classful Advertising
d) Classless Advertising

Answer: a
Explanation: Classful addressing is replaced with classless addressing as a large ratio of the available addresses in a class in calssful addressing is wasted. In classless addressing, one can reserve the number of IP addresses required by modifying the CIDR value and make sure that not many addresses are wasted.

6. First address in a block is used as network address that represents the _____
a) Class Network

b) Entity
c) Organization
d) Codes

Answer: c
Explanation: First address in a block is used as network address that represents the organization. The network address can be found by AND'ing any address in the block by the default mask. The last address in a block represents the broadcast address.

7. In classful addressing, a large part of available addresses are _____
a) Organized
b) Blocked
c) Wasted
d) Communicated

Answer: c
Explanation: In classful addressing, a large part of available addresses are wasted. Thus to solve this classful addressing is replaced with classless addressing where one can reserve the number of IP addresses required by modifying the CIDR value and make sure that not many addresses are wasted.

8. Network addresses are a very important concept of _____
a) Routing
b) Mask
c) IP Addressing
d) Classless Addressing

Answer: c
Explanation: Network addresses are a very important concept of IP addressing. The first address in a block is used as network address that represents the organization. The network address can be found by AND'ing any address in the block or class by the default mask.

9. Which of this is not a class of IP address?
a) Class E
b) Class C
c) Class D
d) Class F

Answer: d
Explanation: Class F is not a class of IP addressing. There are only five classes of IP addresses: Class A (0.0.0.0 to 127.255.255.255), Class B (128.0.0.0 to 191.255.255.255), Class C (192.0.0.0 to 223.255.255.255), Class D (224.0.0.0 to 239.255.255.255), and Class E (240.0.0.0 to 255.255.255.255).

IPv6

1. The size of an IP address in IPv6 is _____
a) 4 bytes
b) 128 bits
c) 8 bytes
d) 100 bits

Answer: b
Explanation: An IPv6 address is 128 bits long. Therefore, 2128 i.e. 340 undecillion addresses are possible in IPv6. IPv4 has only 4 billion possible addresses and IPv6 would be a brilliant alternative in case IPv4 runs out of possible new addresses.

2. The header length of an IPv6 datagram is _____
a) 10bytes
b) 25bytes
c) 30bytes
d) 40bytes

Answer: d
Explanation: IPv6 datagram has fixed header length of 40bytes, which results in faster processing of the datagram. There is one fixed header and optional headers which may or may not exist. The fixed header contains the mandatory essential information about the packet while the optional headers contain the optional “not that necessary” information.

3. In the IPv6 header, the traffic class field is similar to which field in the IPv4 header?
a) Fragmentation field
b) Fast-switching
c) ToS field
d) Option field

Answer: c
Explanation: The traffic class field is used to specify the priority of the IP packet which is a similar functionality to the Type of Service field in the IPv4 header. It’s an 8-bit field and its values are not defined in the RFC 2460.

4. IPv6 does not use _____ type of address.
a) broadcast
b) multicast
c) anycast
d) unicast

Answer: a
Explanation: There is no concept of broadcast address in IPv6. Instead, there is an anycast address in IPv6 which allows sending messages to a group of devices but not all devices in a network. Anycast address is not standardized in IPv4.

5. Which among the following features is present in IPv6 but not in IPv4?
a) Fragmentation
b) Header checksum
c) Options
d) Anycast address

Answer: d
Explanation: There is an anycast address in IPv6 which allows sending messages to a group of devices but not all devices in a network. Anycast address is not standardized in IPv4.

6. The _____ field determines the lifetime of IPv6 datagram
a) Hop limit
b) TTL
c) Next header
d) Type of traffic

Answer: a
Explanation: The Hop limit value is decremented by one by a router when the datagram is forwarded by the router. When the value becomes zero the datagram is discarded. The field is 8-bits wide, so an IPv6 packet can live up to 255 router hops only.

7. Dual-stack approach refers to _____
a) implementing Ipv4 with 2 stacks
b) implementing Ipv6 with 2 stacks
c) node has both IPv4 and IPv6 support
d) implementing a MAC address with 2 stacks

Answer: c
Explanation: Dual-stack is one of the approaches used to support IPv6 in already existing systems. ISPs are using it as a method to transfer from IPv4 to IPv6 completely eventually due to the lower number of possible available addresses in IPv4.

8. Suppose two IPv6 nodes want to interoperate using IPv6 datagrams, but they are connected to each other by intervening IPv4 routers. The best solution here is _____
a) Use dual-stack approach
b) Tunneling
c) No solution
d) Replace the system

Answer: b
Explanation: The IPv4 routers can form a tunnel in which at the sender's side, the IPv6 datagram is encapsulated in to IPv4, and at the receiver's side of the tunnel, the IPv4 packet is stripped and the IPv6 packet is sent to the receiver.

9. Teredo is an automatic tunneling technique. In each client the obfuscated IPv4 address is represented by bits _____
a) 96 to 127
b) 0 to 63
c) 80 to 95
d) 64 to 79

Answer: a
Explanation: Teredo is a technique through which gives the possibility for full IPv6 network connectivity to IPv6 capable hosts which are currently on an IPv4 network. Bits 96 to 127 in the datagram represents obfuscated 1Pv4 address of the IPv4 network.

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4. A link local address of local addresses is used in an _____
a) Isolated router
b) Isolated mask
c) Isolated subnet
d) Isolated net

Answer: c
Explanation: Isolated subnet is very huge sharing network area in this link local address of local addresses is used. A link local address can be configured on any subnet with the prefix “FE80::”.

5. In subcategories of reserved address in IPv6, address that is used by a host to test itself without going into network is called _____
a) Unspecified address
b) Loopback address
c) Compatible address
d) Mapped address

Answer: b
Explanation: In subcategories of reserved address in IPv6, address that is used by a host to test itself without going into network is called loop back address. IPv6 loopback address is 0000:0000:0000:0000:0000:0000:0000:0001. IPv4 loopback address is 127.0.0.1. It’s a reserved address.

6. A few leftmost bits in each address of IPv6 address define its category is called _____
a) Prefix type
b) Postfix type
c) Reserved type
d) Local type

Answer: a

Explanation: Prefix is the bits in the IP address which are placed in leftmost position. A network prefix in IPv6 is given by a CIDR format-liked number at the end of the address.

7. In IPv6 addresses, addresses that start with eight 0s are called _____
a) Unicast addresses
b) Multicast addresses
c) Any cast addresses
d) Reserved addresses

Answer: d
Explanation: In IPv6 address format, the starting bits are specified with eight 0s to represent reserved addresses. These reserved addresses have a certain function pre-defined like the loop-back address is used to test a network card. Reserved addresses cannot be allotted to a machine.

8. Which statement(s) about IPv6 addresses are true?
a) Leading zeros are required
b) Two colons (::) are used to represent successive hexadecimal fields of zeros
c) Two colons (::) are used to separate fields
d) A single interface cannot have multiple IPv6 addresses of different types

Answer: b
Explanation: In order to shorten the written length of an IPv6 address, successive fields of zeros may be replaced by double colons. In trying to shorten the address further, leading zeros may also be removed. Just as with IPv4, a single device's interface can have more than one address; with IPv6 there are more types of addresses and the same rule applies. There can be link-local, global unicast, and multicast addresses all assigned to the same interface.

9. When was IPv6 launched?
a) June 2, 2012
b) June 4, 2012
c) June 5, 2012
d) June 6, 2012

Answer: d

Explanation: IPv6 is the latest version of the Internet Protocol released on 6th June 2012. An IPv6 address is 128 bits long. Therefore, 2128 i.e. 340 undecillion addresses are possible in IPv6.

UDP

1. Which of the following is false with respect to UDP?
a) Connection-oriented
b) Unreliable
c) Transport layer protocol
d) Low overhead

Answer: a
Explanation: UDP is an unreliable, connectionless transport layer protocol that provides message-based data transmission. TCP is an example of connection-oriented protocols.

2. Return value of the UDP port “Chargen” is _____
a) String of characters
b) String of integers
c) Array of characters with integers
d) Array of zero’s and one’s

Answer: a
Explanation: Using Chargen with UDP on port 19, the server sends a UDP datagram containing a random number of characters every time it receives a datagram from the connecting host. The number of characters is between 0 and 512.

3. Beyond IP, UDP provides additional services such as _____
a) Routing and switching
b) Sending and receiving of packets
c) Multiplexing and demultiplexing
d) Demultiplexing and error checking

Answer: d
Explanation: De-multiplexing is the delivering of received segments to the correct application layer processes at the recipients end using UDP. Error checking is done through checksum in UDP.

4. What is the main advantage of UDP?
a) More overload
b) Reliable
c) Low overhead
d) Fast

Answer: c
Explanation: As UDP does not provide assurance of delivery of packet, reliability and other services, the overhead taken to provide these services is reduced in UDP’s operation. Thus, UDP provides low overhead, and higher speed.

5. Port number used by Network Time Protocol (NTP) with UDP is _____
a) 161
b) 123
c) 162
d) 124

Answer: b
Explanation: The Network Time Protocol is a clock synchronization network protocol implemented by using UDP port number 123 to send and receive time stamps.

6. What is the header size of a UDP packet?
a) 8 bytes
b) 8 bits
c) 16 bytes
d) 124 bytes

Answer: a
Explanation: The fixed size of the UDP packet header is 8 bytes. It contains four two-byte fields: Source port address, Destination port address, Length of packet, and checksum.

7. The port number is “ephemeral port number”, if the source host is _____
a) NTP
b) Echo
c) Server
d) Client

Answer: d
Explanation: Port numbers from 1025 to 5000 are used as ephemeral port numbers in Windows Operating System. Ephemeral port numbers are short-lived port numbers which can be used for clients in a UDP system where there are temporary clients all the time.

8. “Total length” field in UDP packet header is the length of _____
a) Only UDP header
b) Only data
c) Only checksum
d) UDP header plus data

Answer: d
Explanation: Total length is the 16 bit field which contains the length of UDP header and the data. The maximum value of the Total length field and the maximum size of a UDP datagram is 65,535 bytes (8 byte header + 65,527 bytes of data).

9. Which is the correct expression for the length of UDP datagram?
a) UDP length = IP length – IP header's length
b) UDP length = UDP length – UDP header's length
c) UDP length = IP length + IP header's length
d) UDP length = UDP length + UDP header's length
View Answer

10. The _____ field is used to detect errors over the entire user datagram.
a) udp header
b) checksum
c) source port
d) destination port

Answer: b
Explanation: Checksum field is used to detect errors over the entire user datagram. Though it is not as efficient as CRC which is used in TCP, it gets the job done for the UDP datagram as UDP doesn't have to ensure the delivery of the packet.

Cryptography

1. In cryptography, what is cipher?
a) algorithm for performing encryption and decryption
b) encrypted message
c) both algorithm for performing encryption and decryption and encrypted message
d) decrypted message

Answer: a
Explanation: Cipher is a method to implement encryption and decryption of messages travelling in a network. It's used to increase the confidentiality of the messages.

2. In asymmetric key cryptography, the private key is kept by _____
a) sender
b) receiver
c) sender and receiver
d) all the connected devices to the network

Answer: b
Explanation: The private key is kept only by the receiver of the message. Its aim is to make sure that only the intended receiver can decipher the message.

3. Which one of the following algorithm is not used in asymmetric-key cryptography?
a) rsa algorithm
b) diffie-hellman algorithm

c) electronic code book algorithm
d) dsa algorithm

Answer: c
Explanation: Electronic code book algorithm is a block cipher method in which each block of text in an encrypted message corresponds to a block of data. It is not feasible for block sizes smaller than 40 bits.

4. In cryptography, the order of the letters in a message is rearranged by _____
a) transpositional ciphers
b) substitution ciphers
c) both transpositional ciphers and substitution ciphers
d) quadratic ciphers

Answer: a
Explanation: In transposition ciphers, the order of letters in a plaintext message is shuffled using a pre-defined method. Some of such ciphers are Rail fence cipher and Columnar transposition.

5. What is data encryption standard (DES)?
a) block cipher
b) stream cipher
c) bit cipher
d) byte cipher

Answer: a
Explanation: DES is a symmetric key block cipher in which the block size is 64 bits and the key size is 64 bits. It is vulnerable to some attacks and is hence not that popularly used.

6. Cryptanalysis is used _____
a) to find some insecurity in a cryptographic scheme
b) to increase the speed
c) to encrypt the data
d) to make new ciphers

Answer: a
Explanation: Cryptanalysis is a field of study in which a cryptographic scheme is intentionally tried to breach in order to find flaws and insecurities. It is used to make sure that the scheme is least vulnerable to attacks.

7. Which one of the following is a cryptographic protocol used to secure HTTP connection?
a) stream control transmission protocol (SCTP)
b) transport layer security (TLS)

c) explicit congestion notification (ECN)
d) resource reservation protocol

Answer: b
Explanation: TLS has strong message authentication and key-material generation to prevent eavesdropping, tampering and message forgery. It has been used since the year 1996.

8. Voice privacy in GSM cellular telephone protocol is provided by _____
a) A5/2 cipher
b) b5/4 cipher
c) b5/6 cipher
d) b5/8 cipher

Answer: a
Explanation: The A5/2 cipher was published in the year 1996 and was cryptanalysed in the same year within a month. It's use was discontinued from the year 2006 as it was really weak.

9. ElGamal encryption system is _____
a) symmetric key encryption algorithm
b) asymmetric key encryption algorithm
c) not an encryption algorithm
d) block cipher method

Answer: b
Explanation: The ELGamal encryption system was made by Taher Elgamal in the year 1985 and is an asymmetric key algorithm. It is popularly used in PGP and other systems.

10. Cryptographic hash function takes an arbitrary block of data and returns _____
a) fixed size bit string
b) variable size bit string
c) both fixed size bit string and variable size bit string
d) variable sized byte string

Answer: a
Explanation: Cryptographic hash functions are used in digital signatures and message authentication codes. The only issue with it is that it returns the same hash value every time for a message making it vulnerable to attackers to evaluate and break the cipher.

1. These ciphers replace a character or characters with a different character or characters, based on some key.
a) Polyalphabetic substitution based
b) Transposition-based
c) Substitution based
d) Mono alphabetic substitution based

Answer: d
Explanation: In mono alphabetic substitution-based cipher, a character is replaced with some other character or multiple characters, based on some key.

2. Encryption is the study of creating and using decryption techniques.
a) True
b) False

Answer: b
Explanation: The statement is false. Cryptography is the study of creating and using encryption and decryption techniques.

3. A type of cipher that uses multiple alphabetic strings.
a) Substitution based
b) Transposition-based
c) Polyalphabetic substitution based
d) Mono alphabetic substitution based

Answer: c
Explanation: These ciphers are similar to that of mono alphabetic ciphers. Multiple strings are used to encode the plain text.

4. An encryption technique with 2 keys is _____
a) Monoalphabetic Cipher
b) Cryptography
c) Private key cryptography
d) Public key cryptography

Answer: d
Explanation: It is called as public key cryptography. It has 2 keys: a private key and a public key.

5. In public key cryptography, a key that decrypts the message.
a) public key
b) unique key
c) private key
d) security key

Answer: c
Explanation: Public key cryptography has 2 keys. They are private key and a public key. The public key encrypts the message. The private key decrypts the message.

6. DES stands for?
a) Data Encryption Standard

b) Data Encryption Statistics
c) Data Encryption System
d) Data Encryption Sequence

Answer: a
Explanation: DES stands for Data Encryption Standard. It was created in 1977 and went into operation from 1990s.

7. Under DES, the data encryption standard took a 64-bit block of data and subjected it to _____ levels of encryption.
a) 64
b) 8
c) 16
d) 4

Answer: c
Explanation: The answer is 16. It was subjected to 16 levels of encryption. DES is the data encryption standard.

8. Triple-DES has _____ keys.
a) 1
b) 2
c) 5
d) 4

Answer: b
Explanation: There are 2 keys in triple DES as well. The private and the public key. It can also have 3 unique keys.

9. Encryption standard that is selected by the US government to replace DES.
a) AES
b) BES
c) CES
d) DES

Answer: a
Explanation: AES is Advanced Encryption Standard. It was selected by the US government. It is used to replace DES.

Asymmetric Key Cryptography

1. Which of the following is not an alternative name for symmetric key cryptography?
a) Secret key cryptography
b) Public key cryptography
c) Conventional encryption
d) Private key cryptography

Answer: b
Explanation: Cryptography is mainly categorized into two types; symmetric key cryptography and asymmetric key cryptography(public key cryptography). Symmetric key cryptography uses only one key for both encryption and decryption.

2. What is the cipher text for the text “GREET HER”, if Caesar Cipher is used(key=3)?
a) KVIIY LIV
b) KVIIX LIV
c) LWJJY MJW
d) JUHHW KHU

Answer: d
Explanation: Caesar cipher is the substitution cipher, which belongs to classical cryptography. Cipher text will be obtained by replacing the plain text letters with letters three places further from them. If further letter is ‘z’, then process will circularly follows ‘a’.

3. What is the cipher text for the message “TAKE ME TO THE PARTY”, id Rail Fence technique is used with two rows?
a) TKMTTEATAEEOHPRY
b) TAKEMETOTHEPARTY
c) TAEKMEOTTHPEARYT
d) YRPHOEEATAETTMKT

Answer: a
Explanation: Rail fence is the transposition technique, that belongs to classical cryptography. First the plain text is written in a sequence of diagonals with defined number of rows, then the cipher text is read off as a sequence of all the rows from starting to end.

4. What are the two broad categories of symmetric key cryptography?
a) Transposition and substitution
b) Classical and modern
c) Stream and Block
d) Classical and Block

Answer: b
Explanation: Symmetric key cryptography has two types; classical and modern. Classical

cryptography again divided into two types; transposition and substitution. Modern cryptography is of two types; stream cipher and block cipher.

5. Which of the following algorithm does not belong to symmetric key ciphers?
a) DES
b) RC4
c) AES
d) Diffie-Hellman

Answer: d
Explanation: Diffie-Hellman is the first asymmetric cipher and well known for its logarithm computations. It is used at its best to transmit the secret key between users for further symmetric encryption of messages.

6. Which of the following is an advantage of symmetric cipher?
a) (N(N-1))/2 keys are required for N people
b) sharing secret key over communication channel
c) Brute force attack for small key size
d) Quick encryption and decryption

Answer: d
Explanation: Quick encryption and decryption is done in symmetric key cryptography. Because, it uses less resources and cipher text length will be small or same as plain text. It encrypts huge amount of data quickly and provides confidentiality.

7. Which of the following is incorrect about symmetric key cryptography?
a) It uses common key for both encryption and decryption
b) It is a secret key cryptography
c) It uses single fixed length key for each algorithm
d) Symmetric key can be combined with asymmetric key to achieve more security

Answer: c
Explanation: An algorithm can make use of number of random keys and the keys can be any size. If the key length is increased, then it will become difficult to crack the key.

8. Which of the following is a disadvantage of symmetric cipher?
a) Quick encryption
b) Less computational power
c) High level of security
d) Transmission of secret key

Answer: d
Explanation: Symmetric key cryptography uses single key to encrypt and decrypt messages. If the secret key is shared through an unsecured channel, then there will be a chance for attacking the key.

9. Which of the following is not an application of symmetric encryption algorithms.
a) Data security
b) Cloud storage
c) User privacy
d) Bitcoin's block chain

Answer: d
Explanation: Unlike data security, cloud storage and user privacy, bitcoin uses elliptic-curve cryptography over symmetric key cryptography. Elliptic curve cryptography not only used for encryption, but also for digital signatures and random generators.

10. Asymmetric ciphers are complex than symmetric ciphers.
a) True
b) False

Answer: a
Explanation: Asymmetric ciphers are much complex and slower than symmetric ciphers. Asymmetric ciphers have longer keys, which are more related to mathematics. As two keys are employed in asymmetric cipher, it is complex than symmetric ciphers.

Digital Signature

1. What can it be called, if an attacker determines the private key of the user, after breaking the signature scheme?
a) Universal forgery
b) Total break
c) Selective forgery
d) Existential forgery

Answer: b
Explanation: Total break is finding private key and Universal forgery is finding signing algorithm. Selective forgery is doing forgery of signature for particular message. Atleast one message can have forgery signature.

2. Which of the following is not a requirement of digital signatures?
a) Easy to produce
b) Easy to recognize

c) Easy to verify
d) Computationally feasible

Answer: d
Explanation: If a digital signature is computationally feasible, then it is very easy for a hacker to attack the signing scheme. He may forge the signature for the new message or change the signature for the present message.

3. Who will be the involving parties in the direct digital signature scheme?
a) source and destination
b) Source and third party
c) Destination and third party
d) Source and destination and third party

Answer: a
Explanation: In general, there will be a third party, who authenticate the digital signatures. But there is no rule that everyone should believe the third party. So, the direct digital signature scheme involves sender and receiver. And receiver knows from where the message is coming using public key of the sender.

4. Which of the following sentence is incorrect in case for digital signatures?
a) Signature key is of signing and public key for verification
b) Public key for verification and signature is for authentication
c) Signature key is for verification and public key for signing
d) Both signing and verification is done by public key

Answer: a
Explanation: In digital signature, private key is the signature key, that is used to create digital signature. And this private key belongs to the signer. Public key belongs to the receiver who receives the message. These two keys are used in digital signature algorithm.

5. What is the advantage of digital signing a hash instead of signing the entire data in RSA?
a) Time saving
b) Security
c) Time saving and computationally less expensive
d) Secured and less time requires

Answer: c
Explanation: RSA uses expressions with exponential, that is modular exponentiation. So, it is difficult to let the large data be signed using modular exponentiation. Hash value of the message is small compared to the whole message. So, it saves time and computation power to use hash to be signed.

6. Which of the following cannot be achieved by the digital signature in symmetric key encryption?
a) Message authentication
b) Data integrity
c) Non-repudiation
d) Security of the message

Answer: d

Explanation: Channel security is not in hands of digital signature, even the secret key is being transmitted between sender and receiver. Security of the message will be depending on the channel that is being used.

7. Which of the following digital signature technique is based on elliptic curve cryptography?
a) ECDSA
b) DSA
c) RSA PSS
d) RSA

Answer: a
Explanation: ECDSA stands for elliptic curve digital signature algorithm. ECDSA has huge acceptance, because it uses small key bit length, elliptic curve cryptography and secured.

8. Which of the following is not a digital signature algorithm?
a) ECDSA
b) DSA
c) RSA – PSS
d) SHA

Answer: d
Explanation: SHA(secured hash function) is the hash algorithm which uses MD4 hash function. ECDSA, DSA and RSA – PSS are the three algorithms in digital signatures. ECDSA stands for elliptic curve digital signature algorithm, RSA – PSS is probabilistic signature scheme. DSA is digital signature algorithm.

9. In which year, NIST proposed Elgamal algorithm in its new DSS(digital signature standard)?
a) 1993
b) 1992
c) 1991
d) 1990

Answer: c
Explanation: After RSA public key algorithm, ElGamal was introduced for digital signatures. But it is

claimed by the government, that this algorithm is too slow, insecure, new and secret to meet the cyptographic standards.

10. A signature function must be performed before the confidentiality function on a plain text in symmetric key digital signatures.
a) True
b) False

Answer: a
Explanation: Confidentiality function involves receivers public key for encryption, and private key for decryption. The sender cannot deceive the receiver when the digital signature function is inside. Because decryption of the message cannot be done by the sender without receiver's private key. And the sender cannot change the digital signature.

Key	AES	DES
Definition	AES stands for Advanced Encryption Standard.	DES stands for Data Encryption Standard.
Key Length	Key length varies from 128 bits, 192 bits to 256 bits.	Key length is of 56 bits.
Rounds of Operations	Rounds per key length: 128 bits - 10 192 bits - 12 256 bits - 14	16 rounds of identical operations.
Network	AES structure is based on substitution-permutation network.	DES structure is based on Feistal network.
Security	AES is de-facto standard and is more secure than DES.	DES is weak, however 3DES (Triple DES) is more secure than DES.

Rounds	The operation rounds involved in AES encryption are Byte Substitution, Shift Row, Mix Column, and Key Addition.	Expansion, XOR operation with round key, Substitution, and Permutation are the rounds used in DES encryption
Size	AES can encrypt 128 bits of plain text.	DES can encrypt 64 bits of plain text.
Derived from	AES is derived from Square cipher.	DES is derived from Lucifer cipher.
Designed By	AES was designed by Vincent Rijmen and Joan Daemen.	DES was designed by IBM.
Known attacks	No known attacks.	Brute-force, Linear crypt-analysis and Differential crypt-analysis.
Encryption	AES can encrypt plain text up to 128 bits.	DES can encrypt 64 bits of plain text.

P-Box:

Function: A fixed transposition cipher that shuffles bits by permuting their positions.

Purpose: Provides diffusion, hiding the relationship between plaintext and ciphertext.

Key: P-boxes are key-less, meaning their operation is fixed and doesn't involve a secret key.

Example: A P-box might take 8 input bits and rearrange them into a specific order, such as.

S-Box:

Function: A substitution cipher that replaces input bits with other bits based on a non-linear transformation.

Purpose: Provides confusion, making it difficult to determine the key from the ciphertext.

Key: S-boxes are dependent on the encryption key, meaning the substitution is not fixed and changes based on the key.

Example: An S-box might take 4 input bits and replace them with 4 output bits based on a lookup table that is part of the key.